NanoElectronics Roadmap for Europe

From Nanodevices and Innovative Materials to System Integration

https://www.nereid-h2020.eu/roadmap

Abstract

The NEREID project ("NanoElectronics Roadmap for Europe: Identification and Dissemination") is dedicated to mapping the future of European Nanoelectronics. NEREID's objective is to develop a medium and long term roadmap for the European nanoelectronics industry, starting from the needs of applications to address societal challenges and leveraging the strengths of the European eco-system. The roadmap will also identify promising novel nanoelectronic technologies, based on the advanced concepts developed by Research Centres and Universities, and potential bottlenecks along the innovation (value) chain. Industry applications include Energy, Automotive, Medical/Life Science, Security, IoT, Mobile Convergence and Digital Manufacturing. The NEREID roadmap covers Advanced Logic and Connectivity, Functional Diversification (Smart Sensors, Smart Energy and Energy for Autonomous Systems), Beyond-CMOS, Heterogeneous Integration and System Design as well as Equipment, Materials and Manufacturing Science.

The project solicits application and technology experts from leading industrial and academic research organizations to participate to General and Domain Workshops, which allow the consortium to better define the technology roadmap according to application requirements and technology evolution. Structured discussion and debate provide the convergence between applications and technologies.

This common work between technology and application experts leads to the early identification of the most promising technologies needing additional R&D actions, which could be very useful for the future electronic products of European companies leading to a strong impact on the European economy and society.

The NEREID Nanoelectronic Roadmap takes into account the specificity of the European industrial and academic landscape, and is very important to better coordinate academic and industrial research for equipment, semiconductors and application developments. It will be used as input for future research programmes at European and National levels in order to join efforts to overcome the main nanoelectronic challenges and put the EU at the forefront of future technological developments.

Acknowledgement

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I. General Introduction

Roadmaps are highly beneficial for all high tech sectors, like Nanoelectronics, to improve links between academic and industrial research, to drive investments, to provide inputs for future research programmes and to coordinate efforts to overcome the main technology challenges.

For more than 20 years, the International Technology Roadmap for Semiconductors (ITRS) has guided the industry to follow Moore's Law, with a constant reduction in device costs and an exponential growth of the semiconductor market. The main role of ITRS has been in providing re-search guidance for the many actors of the semiconductor ecosystem, in synchronizing the technology development and the timely availability of manufacturing equipment and methods and in providing focus on critical bottlenecks.

However, the "technology push" that has been at the base of ITRS has shown in recent years its limits: device size and speed are no longer the only parameters of importance, and system-driven technologies have been considered by the new IRDS Roadmap (International Roadmap for Devices and Systems), focusing on computing systems.

On the other hand, the integration of new functionalities, required by new applications, needs the incorporation of special metrics for technologies that do not necessarily scale according to "Moore's Law", expanding the focus from chips to different kinds of systems. This trend is especially relevant for the European semiconductor industry that has focused on segments of greater relevance for the European industry applications, like Automotive, Industrial and Medical. Therefore, an appropriate kind of roadmap is needed for Europe which focuses on Nanoelectronics with respect to the European abilities and strengths.

The objective of the NEREID project is to elaborate a new roadmap for Nanoelectronics, focused on the requirements of European semiconductor and applications industry to address societal challenges, and the advanced concepts developed by Research Centres and Universities in order to achieve an early identification of promising novel technologies covering the R&D needs all along the innovation chain. The final result is a roadmap for European micro- and nanoelectronics, with a clear identification of medium and long term objectives. The roadmap is divided into main technology sectors: Advanced Logic (including Nanoscale FETs and Memories) and Connectivity, Functional diversification (Smart Sensors, Smart Energy, Energy for Autonomous Systems), Beyond CMOS (Emerging devices and Computing Paradigms), Heterogeneous Integration and System Design, Equipment, Materials and Manufacturing Science, and also includes cross-functional enabling domains.

Understanding the dependencies between short/medium term (e.g. More Moore and More than Moore) and long/ very long term (e.g. Beyond CMOS) activities is also very important to speed-up technology transfer between academia and industry using disruptive technologies leading to possible new large future markets.

The NEREID Roadmap, focused on medium and long term time horizons, is complementary to the AENEAS/ ECS Strategic Research Agenda and the ECSEL MASRIA, which are focusing on shorter terms. NEREID is also planning the evolution of the main Figures of Merit (FoM) vs time horizon for the most promising technologies, which are not included in the ECS SRA. NEREID has some commonalities and is developing joint collaboration with the new International IRDS Roadmap especially in the fields of More Moore, Beyond CMOS and computing systems, but is also complementary to IRDS with very important NEREID activities in the More than Moore domain (e.g. Smart Sensors, Smart Energy, Energy Harvesting), which is a sound European competence, leading to a large diversity of electronic systems useful for many applications. In

the More Moore field, there are also strong interests in Europe for specific activities dealing with very low power systems, leading to possible disruptive applications for instance for future internet of things (IoT) systems, or for application driven performance, e.g. high temperature operation for the automotive industry.

Therefore, the NEREID Roadmap takes into account the specificity of the European industrial and academic landscape, and will be very important to better coordinate academic and industrial research for equipment, semiconductors and application developments, as well as serving as the input for future research programmes at European and National levels in order to coordinate efforts to overcome the main nanoelectronic challenges and put the EU at the forefront of future technological developments.

I.1 Roadmapping Process

The project supported the participation of many application and technology experts, coming from leading research actors in industry and academia, to workshops during which they presented the state-of-the-art. Three major general Workshops and many Domain Workshops (for WPs and Tasks) have been organized with a large participation by European application experts/technology users and technological experts (more than 100 experts) in order to better define the technology roadmap in terms of applications requirements and technology evolution, and discuss the convergence between applications and technologies (s. figure I.1 on next page).

The proposed idea is that the scenarios of evolution of the products/applications will result in performance evolution scenarios for the functions, which could be generic enough to apply to many products. The next step is then to derive, from the evolution of functions, the evolution of the underlying technologies and devices using the expertise of technology experts. Insights on future technology evolution and availability can also prompt new ideas for disruptive products and applications, which are discussed in Domain Workshops and also presented by technology experts during the General Workshops.

This common work between technology and application experts is leading to the early identification of the most promising technologies needing additional R&D activities in order to become useful for the future electronic products of European companies, thus leading to a strong impact on the European economy and society.

The important assets of NEREID are the following:

- the projection of the evolution of many Figures of Merit (FoM) vs time for covering the most promising technologies including novel functionalities
- the understanding of the dependencies between short/ medium term (e.g. More Moore and More than Moore) and long/very long term (e.g. Beyond CMOS) activities
- the strong interaction between application and technology experts, coming from leading research players in industry and academia, especially with the organization of many Workshops.
- the combination of a top-down approach, which is application driven, and a bottom-up one, based on planned technology evolution to prompt new ideas for disruptive products and applications (s. figure I.1 on next page).

I.2 Application domains and Societal benefits of a new European Roadmap

We have proposed to start from the different very important European application areas (Energy, Automotive, Medical/Life science, Security, IoT/Smart connected objects, Mobile convergence, Digital Manufacturing) in order to define the roadmap.

We have therefore invited potential users of the nanoelectronic technologies in the NEREID General Workshops to provide insight on the technology requirements in terms of both performance and timescale for the future applications and/or (generic) functions envisioned by their Companies.

These requests are then used by technology experts for the identification of the most promising technologies and functions that can satisfy the functionalities and performances needed for these different applications.

Societal benefits

Future electronic systems will play a vital role in all of the very important European application areas mentioned above. The world of connected objects and the development of "Smart Everything Everywhere", with huge future markets, imply the development of dedicated technologies like low power devices and the development of many new functionalities for sensing, computing, communicating, energy harvesting, etc.

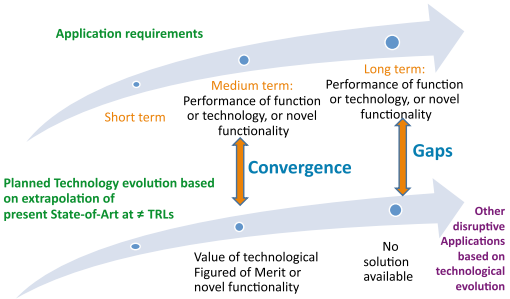


Fig. I.1: NEREID Roadmap

The use of renewable energy sources is becoming one of the most important topics in our society. Among the benefits, it is possible to envisage the development of autonomous, wearable, or even implantable sensor nodes for health applications or environmental monitoring for instance. The development of "green" materials, replacing toxic/rare materials used nowadays, is also of paramount importance for future sustainable systems and society.

On the other hand, the estimated energy saving potential that can be achieved by introducing power electronics into systems is enormous, estimated at more than 25% of the current electricity consumption in the EU countries1. Since power electronics is a key technology in achieving a sustainable energy society, the demand for power electronics solutions will show significant growth in the coming decades.

In the health sector, the strong incidence of chronic diseases, such as cancer, cardiovascular diseases, obesity, diabetes, autoimmune and psychiatric diseases will increase the demand for diagnostic devices (activity trackers, body monitors and multi-parameter real-time sensing) and for most devices a low-cost, portable and fast diagnostic solution does not exist in the market yet. Moreover, similar devices could also serve to detect the incidence of health hazards caused by pollution (air quality, water and food monitoring, …) and address rising concerns about health and well-being. These emerging medical devices (wearable sensors, implantable sensors and others) would benefit healthcare facilities and simplify the acceptance of personalized, more-efficient medicines.

The connectivity functions will be everywhere in the future connected world, starting from the physical world, e.g.the things and the persons, the autonomous objects, factory 4.0, to the cloud.

An early consideration of all these trends, which have been taken into account in the NEREID Roadmap, will be beneficial to the EU. NEREID will lead to disruptive technologies and applications and many new markets, strengthening the international position of the European economy and having a great potential impact on the European society.

I.3 Interactions with other international activities

The activities of NEREID account for the international context of roadmapping through the Advisory Board that include personalities involved in USA and Asia in similar activities. They are proving systematic feedback about the coherence and complementarity of NEREID with the global context, while constructively recognizing the European focus on priorities, specific to NEREID.

On the other hand, NEREID has concretely started and implemented a series of actions of reciprocal benefits with the International Roadmap of Devices and Systems (IRDS) supported by IEEE organization. In fact, almost simultaneously with the launch of NEREID, in May 2016, IEEE announced the formation of the IRDS under their sponsorship to address the mapping of the ecosystem of newly reborn electronics industry. The migration from ITRS to IRDS is proceeding seamlessly, with all reports produced in the past by the ITRS 2.0 representing the starting point, and including contributions and groups from USA, Asia and Europe (i.e. an international dimension). The first IRDS Roadmap (2017) has been published in June 2018. This was a unique opportunity for NEREID to forge a partnership with IRDS and have reciprocal participation in meetings, and building a vision about the future of Nanoelectronics, to which each initiative contributes with its specific strong points. Of particular importance is the concrete actions taken to compare roadmaps between NEREID and IRDS in the following fields, in which the interests of the two initiatives overlap:

- Systems and Architectures: Cloud computing, IoT, Smartphone, Cyber Physical systems,
- Outside System Connectivity: RF & Analog & Mixed Signal, Photonic Interconnects,
- Beyond CMOS: Emerging memory and storage devices, Emerging information processing and logic devices, Emerging devices for functional diversification, Interface between emerging devices and novel computing architectures/paradigms,
- Metrology,
- Yield,
- More Moore: Logic technology

NEREID was also in charge of the "long term Grand Challenges" of the IRDS Roadmap, which has been published in the Executive Summary of IRDS.

Therefore, NEREID has also developed collaboration with, and is in part complementary to, the IRDS in the Europe-led More than Moore domain (e.g. Smart Sensors, Energy, Energy Harvesting) leading to beyond-computing systems.

With its mid/long term focus, the NEREID Roadmap is also complementary to the European ECSEL ECS Strategic Research Agenda, which is focusing on shorter term horizons.

1 Quotations from the CATRENE White Book: Public Final Report of the E4U Project Electronics enabling effi energy usage, funded by the European Commission's ICT programme in FP7 (project no. 224161), 2009 (2) J. Popovic, Gerber et al, „Power electronics enabling efficient energy usage: energy savings potential and technological challenges „ IEEE Transactions on Power Electronics, vol. 27, no. 5, pp. 2338 -2353, May 2012

II. Nanoelectronic Technology Sectors

Overview on Technology Sectors and their Main Concepts

The NEREID roadmap is structured by the following nanoelectronic technology sectors, which are covered in the following Chapters (II.1 to II.8). Within all these technology sectors the roadmap follows a fixed structure which addresses the technologies' relevance, its competitive value, its vision, its scope and ambition, its synergies with other topics and its main concepts. Finally, each chapter ends with some recommendations for the technology sector.

On this page, all technology sectors are listed with all the main concepts that have been considered in the NEREID roadmap.

II.1 Advanced Logic and Memories (NEREID TASK 3.1)

- Nanowires
- FinFET
- FD-SOI
- Negative Capacitance FET (NCFET)
- Carbon Nanotubes (CNTFET)
- Memories, Concept 1 - OxRAM:
- Memories, Concept 2 - CBRAM
- Memories, Concept 3 - PCM
- Memories, Concept 4 - MRAM
- 3D sequential integration
- Reliability

II.2 Connectivity (Wireline and Wireless) (NEREID TASK 3.2)

- The Outdoor Wireless Applications
- The Outdoor Wireline Applications
- The Indoor Wireless Applications
- The Indoor Wireline Applications
- The Device to Device Wireless Applications
- The In Package/Device Photonics Wireline Applications

II.3 Smart Sensors (NEREID TASK 4.1)

- Sensor's for car internal system performance
  - Motion and Pressure sensors
  - Advance Driver Assistance System (ADAS)
    - Image Sensors-, Radar LiDAR- and Infrared sensors
- Environmental monitoring:
  - Gas and Particulate Matter sensors
  - Sensors for medical and healthcare
  - Physiological signal monitoring
  - Implantable sensors
  - Molecular diagnostics

II.4 Smart Energy (NEREID TASK 4.2)

- Si based power devices
- GaN-devices and substrates
- SiC-based substrates
- Alternative Wide Bandgap Semiconductors

II.5 Energy for Autonomous Systems (NEREID SubTASK 4.2.11)

- Mechanical EH: Electrostatic transduction
- Mechanical EH: Piezoelectric transduction
- Mechanical EH: Electromagnetic transduction
- Thermal energy harvesting
- Photovoltaic Energy Harvesting
- RF energy harvesting/wireless power transfer
- Energy storage - Microbatteries
- Energy storage - Microcapacitors
- Micro-Power Management

II.6 System Design and Heterogeneous Integration (NEREID Workpackage 5, WP5)

In this chapter, the main concepts are classified by connecting the three applications

- Automated Driving;
- Implantable Devices;
- Environmental Monitoring and Wearable Systems,

with different elements of Application-Aware Hardware-Software-Co-Design. These Elements comprise Functionalities, Implementation Qualities and Criticalities and Needs.

II.7 Equipment and Manufacturing Science (NEREID Workpackage 6, WP6)

- More Moore
- More-than-Moore
- Manufacturing Science

II.8 Beyond-CMOS – Emerging devices and Computing Paradigms (NEREID Workpackage 2, WP2)

- Steep slope switches: Tunnel FETs
- Neuromorphic circuits and computing
- Spintronics
- Quantum Photonics
- Phonon, Brownian and nano-opto-mechanical computing

II.1 Advanced Logic and Memories

Executive summary

The historical trend in micro/nano-electronics over the last 40 years has been to increase both speed and density by scaling down the size of electronic devices, together with reduced energy dissipation per binary transition, and to develop many novel functionalities for future electronic systems. We are facing today dramatic challenges for More Moore and More than Moore applications: substantial increase of energy consumption and heating which can jeopardize future IC integration and performance, reduced performance due to limitation in traditional high conductivity metal/low k dielectric interconnects, limit of optical lithography, heterogeneous integration of new functionalities for future nanosystems, etc.

Therefore many breakthroughs, disruptive technologies, novel materials, and innovative devices are needed in the next two decades.

With respect to the substantial reduction of the static and dynamic power of future high performance/ultra low power terascale integration and autonomous nanosystems, new materials, ultimate processing technologies and novel device architectures (FD-SOI, FiNFET, Nanowire FET, Carbon Nanotube FET, Ferroelectric Gate FET with Negative Capacitance, Non-charge-based Memories, 3D integration) are mandatory for different applications using ultimate CMOS, as well as new circuit design techniques, architectures and embedded software.

This section will focus on the main trends, challenges, limits and possible solutions for future high performance and ultralow power nanoscale devices in the CMOS arena.

Relevance and competitive value

What are the advantages of the chosen technologies (concepts) compared to others?

During decades, Moore's law was the main driver of the CMOS world, and most of the electronic industries were scaling the CMOS area by a factor 2 every 2 years. At the 32/28 nm node, the industry introduced the first CMOS revolution by leaving the classical bulk CMOS integration to shift to thin-film devices for improved electrostatic control.

In this way, STMicroelectronics introduced the 28FD-SOI, and companies like INTEL, Samsung and TSMC have shifted to FinFET technologies and are continuing down to the 10 and 7 nm node. In this context, the CMOS world is facing a second revolution, as the famous Moore's law slows downs because cost and complexity of scaling are increasing faster than economic advantages. The technology-push approach that has driven semiconductor evolution is slowing down, while the market is shifting to a more application-driven approach. This implies that technology differentiation is becoming again a critical issue for semiconductor actors.

Vision

For future, reliable, high performance and/or low power ICs and systems, new materials (strained semiconductors, SiGe, Ge, III-V, 2D, 1D, Ferroelectric, Carbon), ultimate processing technologies and novel device architectures (FD-SOI, FinFET, Nanowire FET, CNTFET, NCFET, Non-charge-based Memories, 3D integration) are required.

In the field of alternative memories, PCRAM, RRAM, MRAM, or Ferrolectric RAM will be useful for pushing the limit of integration and performance beyond those afforded by present Non-Volatile, DRAM and SRAM memories.

3D sequential processes could also be used for the integration of these future high performance sustainable, secure, ubiquitous and pervasive systems, which will be of high added value for many applications in the field of detection and communication of health problems, environmental quality and security, secure transport, building and industrial monitoring, entertainment, education, etc.

Scope and ambition

We have chosen some core technologies that we think are the most promising for many future applications in order to overcome the number of challenges we are facing for future ICs, in particular:

- High performance
- Low/very low static and dynamic power consumption
- Device scaling
- Low variability
- Affordable cost

Considering these challenges, the following nanodevices and technologies have been considered as very relevant for future Nanoscale FETs:

- FD (Fully Depleted) SOI (Silicon-On-Insulator) MOSFET: for low power applications and low variability
- FinFET (or Trigate FET): for high performance and/or low power applications
- Nanowire FET: for high performance and low power applications and ultimate integration
- CNTFET/Carbon NanoTube FET: for very fast and possibly ultimately scaled transistors for logic applications, with self-assembly based fabrication
- NCFET/Negative Capacitance FET : for very low power application using steep subthreshold slope
- Non-charge-based Resistive Memories or alternative charge-based Memories: to replace charge-based memories using PCRAM (Phase Change RAM), RRAM (Resistive RAM using a nanofilament), MRAM (Magnetic RAM, especially STT/Spin Transfer Torque MRAM), or FeRAM or FeFET (using the polarization of a ferroelectric material)
- Sequential 3D integration: for increasing device integration (transistors, memories, sensors, etc.) using 3D stacking
- The roadmap also covers the future modelling and characterization tools needed for developing these future devices and technologies.

Main Concepts

- Nanowires
- FinFET
- FD-SOI
- Negative Capacitance FET (NCFET)
- Carbon Nanotubes (CNTFET)
- Memories, Concept 1 - OxRAM:
- Memories, Concept 2 - CBRAM
- Memories, Concept 3 - PCM
- Memories, Concept 4 - MRAM
- 3D sequential integration
- Reliability

Nanowires

The evolution of MOSFETs is shown in Fig. II.1, starting from plane device to FinFET, ending by Nanowire FET, which could be the best device due to the following advantages:

- Advantageous carrier transport with optimized volume inversion: high transconductance gm and driving current I_{on}
- Wrap-gate geometry and small nanowire diameter: large number of electrons, low output conductance g_d, reduced short channel effects DIBL (Drain Induced Barrier Lowering) and charge sharing, low I_{off}.

Key research questions/issues

- What performance (I_{on}, I_{off}, gm, ft/f_{max}, NF) can be achieved in different materials and geometries?
- How can different materials/geometries be manufactured at large scale?
- Evaluation of interface and dielectric quality from HCI and PBTI measurements
- Investigations of variability for 10 nm nanowire diameter/gate length transistors
- Circuit/technology co-design in 3D transistor architectures
- Integration strategies for III-V technology on a Si platform

Medium Term [+5 years]

- Available data suggests that the best performance (lowest Ioff, highest Ion, highest gm, etc) is obtained for Si, Ge, and III-V nanowires. Hybrid III-V/SiGe channel technology has been demonstrated as well as III-V gate stacks with Dit<10^{12} cm^{-2}. Transistor data is available for <10^{-15} nm In(GaAs) diameter

Long Term [+10 years]

- Current status includes first demonstrations of SRAM cells and first nanowire amplifiers designed in complex 3D geometries. A maturing technology will enable circuit implementation
- With current efforts on TMD materials synthesis, it is likely that the technology will mature and contribute to the roadmap

Application needs & Impact for Europe

- Extend the roadmap for CMOS scaling based on improved electrostatic control and increased drive current
- Meeting the low-power demand for IoT applications
- Enhance the CMOS RF-properties by (III-V) materials integration
- Increase performance in mixed-domain by increase in f_t/f_{max}
- Provide opportunity for efficient mmWave front-ends combined with high-speed digital logic
- Electrostatic control provided by nanowires/nanosheets critical for TFET implementation
- Low power operation suitable for Neuromorphic computing and Quantum Technologies

Medium Term [+5 years]

- Tailoring of Si and Ge nanowire transistors to meet the demands of IoT.
- Introduction of hybrid III-V/Si(Ge) and/or all III-V technology for high-performance applications (both RF/mmWave and mixed-mode)

Long Term [+10 years]

- Integration of high-speed logic and high-performance RF front-ends using III-V technology combined with CMOS and possible TFETs

Technology and design challenges

- Challenges in terms of 3D processing in complex geometries at 10 nm Lg
- Evaluation and reduction of parasitics in 3D transistors at 10 nm Lg
- Understanding and reduction of thermal effects in 3D transistors at 10 nm Lg (heating, reliability …)
- Strain engineering (processing, characterization etc) at the 10 nm length scale
- 3D vertical transistor stacking to reduce area (vertical/lateral channels)
- Strategies for co-integration of various types of transistors (Si, Ge, III-V, CNT) in manufacturable CMOS processes
- Transistor and circuit co-design and optimization in complex 3D structures
- Introduction of Ferroelectric gate stacks to boost Ion

Medium Term [+5 years]

- Maturing of the process technology for Si, Ge and III-V nanowires to meet the requirements of IoT and high-performance applications
- First demonstration of nanowire circuits with competitive/high performance

Long Term [+10 years]

- Circuit layout in complex 3D architectures with minimized parasitics
- Improved materials and process control of 2D materials

Other issues & challenges, interaction with other areas

- Nanowire transistors provide the electrostatic control required for TFETs
- The electrostatic control in nanowires and sheets will allow for reduction of off-state leakage to meet IoT requirements
- The high gm and self-gain make nanowire transistors promising for millimeter wave applications (connectivity)
- A selection between nanowires and FinFETs is likely
- Technology suitable for Neuromorphic Computing and Quantum Technologies

Medium Term [+5 years]

- The technology development will follow point 1a-c

Long Term [+10 years]

- The technology development will follow point 1a-c

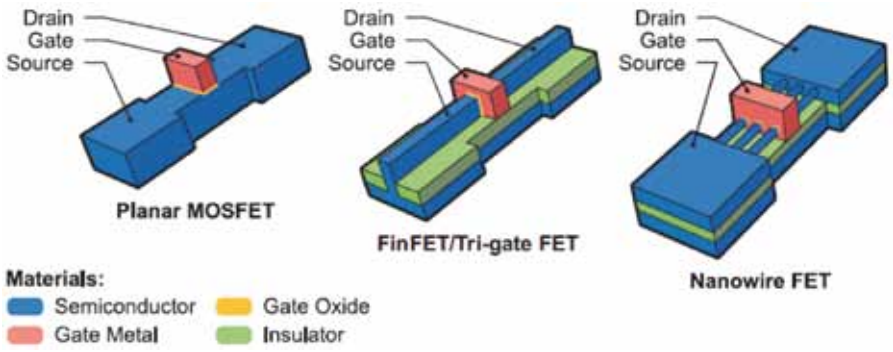


Fig. II.1.1: Evolution of MOSFETs from planar structure to nanowire

Nanowires

Competitive situation of Nanowires

Nanowire FET can be considered as the best FETs for the ultimate integration of CMOS devices with the best performance and lowest power consumption for the 0X technology nodes.

Recommendations for Nanowires

- Identify the best material and geometry options for logics (high-speed as well as low-power)
- Develop millimeter wave front-ends with III-V MOSFETs (applications for communication, radar)
- Develop transistor/circuit co-design strategies for mixed and mmW applications
- Consider the 3D aspects of processing (stacking, vertical integrations etc)
- The electrostatics and heterostructure design options provided are beneficial for TFETs

Definition of FoMs or planned evolution

FoM / Planned Evolution	2023	2026	2029	2033
I_{on} I_{off} g_m f_t/f_{max} NF	Ion 650 µA/µm (normalized to periphery) > 3 mS/µm gm (normalized to periphery) < 1 nA/µm Ioff > 500 GHz fmax	g_m > 3.6 mS/µm	g_m > 4.3 mW/µm	g_m > 5.1 mS/µm

FD-SOI

Fully Depleted Silicon On Insulator, or FD-SOI, is a planar process technology that relies on two primary innovations. First, an ultra-thin layer of insulator, called the buried oxide, is positioned on top of the base silicon. Then, a very thin silicon film implements the transistor channel. Thanks to its thinness, there is no need to dope the channel, thus making the transistor Fully Depleted. The combination of these two innovations is called "ultra-thin body and buried oxide Fully Depleted SOI" or UTBB-FD-SOI. FD-SOI technology enables control of the behavior of transistors not only through the gate, but also by polarizing the substrate underneath the device, similarly to the body bias available in Bulk technology. As the slowing of Moore's law signals the beginning of "Smart Everything", each FD-SOI process node can be a long lasting technology with differentiated options (RF, Mixed signal, Ultra Low Power, Embedded Memories, sensors…). The challenges and needs will be mainly focused on their ultra-low power possibilities to reduce as much as possible the supply voltage and improve the energy efficiency.

Competitive situation of FD-SOI

FD-SOI MOSFETs can be considered as the best FETs planar devices for low power applications, harsh environments (radiation, temperature), and they are also very interesting for analog and RF applications. While FinFET is dedicated to high performance computing and high end application processor, FD-SOI is more dedicated to consumer applications, mid-range smartphones, IoT, wearables and sensors.

GLOBAL RECOMMENDATIONS for FD-SOI

From technological point of view, performances can be boosted also with breakthrough approaches like sSOI, monolithic 3D integration (e.g 28 nm/28 nm) or new materials without device scaling. From device architecture point of view, FD-SOI technology can suit 14 nm & 10 nm nodes and can be replaced by FinFET or Nanowires for 7 nm and below.

- Improve Performances with strain techniques & materials
- Develop differentiated options (RF, Embedded Memories, Imaging or sensors) on FD-SOI (applications for automotive, IoT, smart sensors…)
- Integration of FD-SOI with NVM (like PCM, OXRAM, FeFET…)
- Develop ULP design (V_d <0,4 V) for IoT market (wearable, medical…)
- FD-SOI and 3D integration can respond to future neuromorphic and quantum computing approaches

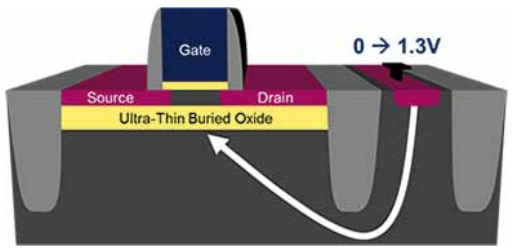


Fig. II.1.2: FD-SOI (source: www.st.com)

Definition of FoMs or planned evolution

FoM / Planned Evolution	2023	2026	2029	2033
I_{eff}/I_{off}	I_{eff} 470/420 µA/µm @10 nA/µm I_{off}	I_{eff} 470/420 µA/µm @10 nA/µm I_{off}	Differentiation through options	Differentiation through options
Variability (Avt)	< 1 mV.µm	< 0.9 mV.µm	< 0.8mV.µm	< 0.8 mV.µm
V_{dd} (logic)	< 0,7 V	< 0,65 V	< 0,6 V	< 0,6 V
Subthreshold slope	< 70 mV/dec	< 65 mV/dec	< 65 mV/dec Introduction of sub-60mV/dec technologies	< 60 mV/dec Introduction of sub-60mV/dec technologies

FD-SOI

Key research questions/issues	*Medium Term [+5 years]*	*Long Term [+10 years]*
• Improving performances for sub-14 nm nodes (strain technologies for Higher drive current)	• Introduction of dual stressors • on sSOI wafers	• More efficient dual stressors • on sSOI wafers
• Structure evolution (Si & BOX thickness reduction challenges) for electrostatic control for sub 14nm node	• T_{si} <6 nm • T_{box} <15 nm	• T_{si} <5 nm • T_{box} <10 nm
• Evolution of planar FD-SOI to multi-gate structure (nano-sheet) with at least 2 conductive channels	• Development of planar nanosheet devices (2 channels)	• More than 3 channels (multi stacks)
• Design evolutions exploiting back biasing techniques	• ULP IoT dedicated design V_d < 0,5 V	• ULP IoT dedicated design V_d <0,4 V
• Evolution of FD-SOI platform to new materials (GeOI, III-V OI) and sequential 3D integration	• sSOI, SiGeOI with high Ge content, sequential 3D	• sequential 3D sSOI / GeOI / III-V-OI for RF
• FD-SOI Logic & embedded flash memories for microcontroller applications / Automotive applications	• Development of embedded flash memories (PCRAM, …)	• New flash memories, innovative selector device
• FD-SOI with Ferroelectric (FeFET)	• Development of FeFET for NVM	• FeFET for NVM
• Electrical characterization of small scale devices (transport, capacitances, local strain impact…)	• New techniques for short devices transport characterization	• Evolution to Ballistic transport

Application needs & Impact for Europe	*Medium Term [+5 years]*	*Long Term [+10 years]*
• low power applications	• Consumer, IoT, Automotive…	• Automotive smart sensors / imaging computing
• Ultra-Low Power devices for IoT (V_{dd} <0,4V)	• Application to wearable devices	• Application to medical devices
• Harsh environment resistant devices	• Spatial applications	• Spatial applications
• FD-SOI Logic & embedded flash memories for microcontroller applications / Automotive applications	• Automotive, IoT	• Automotive, IoT
• FD-SOI development for Analog and RF applications and integration with bipolar devices for high speed devices	• High speed Datacom	• High speed Datacom
• Application of FD-SOI for Innovative sensors (use of FD-SOI design for sensing)	• Concept of new sensors with FD-SOI (Imaging, pH sensing, gas sensing…)	• Applications to integrated and low power Gas sensing, biosensing, Autonomous Imaging
• Beyond CMOS devices co-integration w/ CMOS (Quantum devices – eg: Qbit)	• Development of Quantum devices	• Development of Quantum systems
• FD-SOI for neuromorphic circuits design challenges	• 3D integration for neuromorphic designs for processors	• 3D integration for neuromorphic designs

Technology and design challenges	*Medium Term [+5 years]*	*Long Term [+10 years]*
• Integration of Strain SOI substrates: processing of tensile strain for NMOS & compressive strain for PMOS	• Local strain N & P MOS	• Local strain N & P MOS
• Compatibility with flash memories process (as eg in BEOL)	• Reliable and energy efficient embedded memory	• Reliable and energy efficient embedded memory
• FD-SOI design for ultra-low power (V_{dd}<0,4V)	• Subthreshold circuits	• Circuits with sub-60 mV/dec devices
• Evolution of FD-SOI co-integrated with Tunnel FET option	• Development of solutions for sub-60 mV/dec devices	• Development of solutions for sub-60mV/dec devices
• Thermal management/self-heating mitigation with 3D integration	• Passive Local cooling solution	• Low cost Passive Local cooling solution
• Integration with new materials (SiGe, High Ge content) and future III-V materials (logic applications)	• High Ge conc. SiGeOI	• 3D III-V OI circuits
• New material for differentiator: III-V OI for photonic	• Development of Co-integration of CMOS with Si-photonic	• Development of Co-integration of CMOS with Si-photonic

Other issues & challenges, interaction with other areas

- Link with II.8: enabler for neuromorphic computing/ quantum computing
- Link with II.3-5: sensors+ CMOS co-integration enabler
- Link with II.6: need for understanding system level benefit of 3D sequential options
- Link with II.7: development of strain silicon layers, low T processes, wafer bonding for new material on insulator, low temperature epi, gate stack materials/ interfaces development for low T for 3D technologies and new materials integration

FinFET

FinFETs are presently the most advanced nanodevices especially for high performance applications. They are using a trigate structure for improving the driving current and the control of electrostatic effects, as show below:

Competitive situation of FinFET

FinFET is the current workhorse device for advanced Si CMOS technologies and is current best option for the high performance space. It can also cover a part of the low power/low cost space.

Recommendations for FinFET

- Develop co-integration of different channel materials
- Develop low thermal cycle finFETs for sequential integration
- Develop low contact resistivity and high strain solutions
- Improve finFET analog performance
- Develop finFETs as devices for quantum computing

Key research questions/issues

- subthreshold slope control to less than 70mV/dec at very short gate length (<14 nm)
- improved device performance (I_{on}/I_{eff} at given I_{off}) while scaling the gate length and pitch
- control of parasitic capacitances at scaled dimensions
- Variability control at very scaled dimensions

Medium Term [+5 years]

- innovation needs to continue in the following areas: contact resistivity, conformal doping, dopant activation above solid solubility limit, low k or air spacer; HKMG scaling and multi-V_t; high mobility channels; channel strain enhancement; integration of taller fins;
- understand under what conditions nanowires will outperform finFETs;
- Co-integration with other device architectures or between 2 channel materials
- 3D sequential integration with other devices

Long Term [+10 years]

- finfet is becoming a mature device architecture, on the longer term all optimization knobs may be already understood.
- 3D sequential integration with other devices

Application needs & Impact for Europe

- current workhorse device for Si CMOS technologies
- current best option for high performance space
- currently can cover part of the low power/low cost space

Medium Term [+5 years]

- high performance space

Long Term [+10 years]

- high performance
- can be considered for quantum computing as qbits
- Specialty sensors

Technology and design challenges

- No single device/material able to replace Si CMOS; Co-integration of finFET with other device architectures or between different channel materials will be key
- Improve finFET analog performance

Medium Term [+5 years]

- develop finFETs that can be processed at low T;
- develop finFETs that can withstand a long thermal cycle for 3D sequential integration;
- develop integration flows for multiple channel materials and strain(e.g. Si, SiGe, Ge, III-V on Si or SRB)

Long Term [+10 years]

- develop co-integration schemes between finFETs and nanowires/nanosheets

Other issues & challenges, interaction with other areas

- manufacturing processes and integration will become very complex; working with increased aspect ratios will be key
- system level studies to decide what are the best devices to be co-integrated and in what way, for a given application

Medium Term [+5 years]

- Manufacturing processes to be developed are same as in Key research questions/issues and Technology and design challenges

Long Term [+10 years]

- Manufacturing processes to be developed are same as in Key research questions/issues and Technology and design challenges

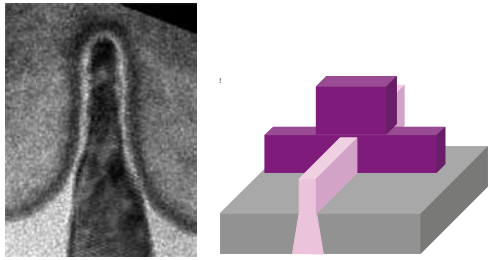


Fig. II.1.3: FinFET realized on bulk Si substrate

Definition of FoMs or planned evolution

FoM / Planned Evolution	2023	2026	2029	2033
Ieff at fixed Ioff (normalized): 1	1.2	1.3	1.45	1.55
CV/I (normalized): 1	0.75	0.7	0.55	0.5
S (mV/dec): 65	67	69	71	75
min achievable I_{off}	<10 pA/um	<10 pA/um	<10 pA/um	<10 pA/um
Avt	<1 mV.um	<1 mV.um	<0.8 mV.um	<0.8 mV.um

Negative Capacitance FET (NCFET)

NCFETs ("Negative Capacitance" FETs) also have the potential to break the 60 mV/dec subthreshold slope limit but rely on another mechanism than TFETs. NCFETs have the same structure as MOSFETs except that a ferroelectric thin film is inserted between the dielectric and the gate. The ferroelectric material has a nonlinear polarization response to an applied electric field, with ionic dipoles switching when a coercive field Ec is reached. Measured in a metal-ferroelectric-metal stack, it shows hysteretic characteristic with residual polarization Pr (or -Pr) at zero applied field. Used in the transistor gate stack, the ferroelectric layer can lead to abrupt turn-on of the transistor from depletion to inversion during polarization switching, the polarized layer behaving as negative differential capacitance (i.e., opposite-polarity charge-electric field characteristic) during this transient. The polarization acts as a voltage shifter or a voltage amplifier, with the voltage seen by the transistor channel exceeding the applied gate voltage. If designed properly, this "negative capacitance" transient could possibly be stabilized by the series dielectric and depletion capacitance, leading to a hysteresis-free sub-60 mV/dec operation.

Ferroelectricity was for a long time studied in perovskites, which are not compatible with CMOS processing. The emergence of Hafnium based ferroelectric layers since 2011 opens the door to standard CMOS compatibility and enables better scaling and integration to MOSFETs or FinFETs, therefore placing the NCFET as potential candidate for continuation of the scaling roadmap

Competitive situation of Negative Capacitance FET

A lot of research efforts are dedicated to the Negative Capacitance FETs. NCFET are plausible candidates to enter the logic scaling roadmap, in particular in the lower power range, where the steep slope allows to reduce Vdd while preserving the drive current.

Recommendations for Negative Capacitance FET

- Identify the maximum switching speed from dedicated RF measurements
- Identify from TCAD and modelling the optimal dimensions, in particular the coercive field and residual polarization for ultra scaled FETs
- Develop thin Hafnium based Ferroelectric layers with low coercive field and target polarization
- Develop understanding of the impact of traps and develop design and technology mitigation strategies.
- Develop compact models and design tools and evaluate the power-performance on real design contexts
- Investigate the impact of hysteresis at design level
- Investigate the scaling potential of the device

Other issues & challenges, interaction with other areas

- Suppression of trapping in the ferroelectric layer.
- Maintaining ferroelectric layer parameters during operation due to phase and temperature changes.
- Variability, reliability.
- Link with WP2: potential enabler for neuromorphic computing
- Link with WP6: development of strain silicon layers, low T processes, gate stack materials/interfaces development

Medium Term [+5 years]

Long Term [+10 years]

Key research questions/issues

- Speed: what is the minimum FE layer polarization switching speed. Critical question for applications in logic circuit as it determines the maximum frequency of operation.
- Maximum frequency reported in literature ranges from ms to ps.
- Expected SS improvement over equivalent MOSFET or FinFET and benefit at circuit level.
- Proof that hysteresis free and sub-60 mV/dec operation are possible (stabilized capacitance behavior). If not, is it possible to use it with hysteresis and what is the impact on circuit (active power, speed, variability).
- Limit of drive current: Although polarization amplifies the gate voltage and improves SS, the equivalent oxide thickness (EOT) is increased by the FE layer thickness compared to MOSFETs, this might lead to reduced Ion in the high performance range.

Application needs & Impact for Europe

- NCFET is a potential candidate to continue the logic scaling roadmap if included in FinFET gate stacks at aggressive nodes. It could improve the Ion/Ioff ratio from low power to standard Vt flavors, and allow reducing V_{dd} while preserving performance. Compared to FinFETs, its weaker design space is the high performance at high Vdd range.
- NCFET could also be a candidate to expand technologies at more relaxed dimensions such as in SOI and bulk planar 28 nm to 65 nm nodes, by improving performance and reducing power without area scaling and at lower cost than aggressive nodes.

Technology and design challenges

- Fabrication of thin Hafnium based (in $Hf_xZr_{1-x}O_2$ and HfAlO) ferroelectric layers. Challenges of ferroelectric phase formation: strain, doping and anneal effect on Orthorhombic fraction, polarization barrier, crystallization. Experiment supported by ab-initio studies.
- Identification of the adapted coercive field and residual polarization for logic application and the feasibility to obtain them in fabricated layers : Ec need to be lower than in FE memories while Pr needs to be sufficient but designed according to the transistor available free charge.
- Capacitance matching: the FE layer, the oxide/interface dielectric and the depletion capacitance have to be properly designed (capacitance matching) to have FE switching in depletion and to reduce the hysteresis.
- Polarization switching dynamics and frequency limit: understanding nucleation and domain wall propagation.
- Multi-domain or uni-domain ferroelectric layers : need and feasibility to make FE-layers with uni-domain nucleation.
- Impact of depolarization field: need and drawbacks of the depolarization.
- Footprint and scaling challenges: 2D field distribution, gate length versus gate stack scaling, ultimate FE scaling.

Definition of FoMs or planned evolution

FoM / Planned Evolution	Device level metrics	Circuit metrics
Too early stage technology to plan FoMs evolution,	Average SS over 3 to 4 decades of subthreshold current (forward and reverse). Minimum SS in forward and reverse Vgs sweeps (SS_{min} = 0 if abrupt switching). I_{on}/I_{off} over V_{dd} and V_t ranges (impact of V_{dd} and V_t on FE operation). Negative DIBL, negative differential resistance.	Logic active power consumption due to hysteresis. SRAM stability with hysteresis.

Carbon Nanotubes (CNTFET)

Carbon nanotubes (CNTs) are hollow cylinders composed of one or more concentric layers of carbon atoms in a honeycomb lattice arrangement, with a typical diameter of 1–2 nm. Depending on the arrangement of the carbon atoms, the CNTs can be either metallic or semiconducting, and are considered both for interconnect or as field effect transistors (FETs). The main expected benefits as field effect transistors over Silicon based devices are the following:

- The low-field mobility is very high in carbon nanotubes, much higher than in any other materials. This is due to the extreme reduction of scattering effects because there is no dangling bonds and surface states at the surface (perfect covalent carbon bonds), and because the transport is one dimensional. Ultimately this could lead to much higher drive current than in silicon based devices at same geometries, enabling higher speed, or reduction of the operating voltage and hence lower active power.
- The tube diameter is controlled by chemistry not by printing, allowing to reduce the body dimension beyond what is achievable for FinFETs and nanowires, that are defined by lithography. This ultra-scaled body leads to higher gate to channel coupling and better electrostatic control at short gate length. The small size also allows the fabrication of aligned arrays with high packing density.
- The intrinsic capacitance is a quantum capacitance related to the density of states and independent of electrostatics. The device capacitance could hence be much lower than the FinFETs gate to channel capacitances, reducing the switching energy.

Competitive situation of Carbon Nanotubes

The main research centers on CNTs are the university of Stanford and IBM. CNT have a lot of potential but the problem of source/drain contacts and the problem of variability due to metallic CNTs and to doping or ambipolarity need to be overcome and at the moment lower their chance to be competitive as field effect transistors. Their use in optical and biosensors applications is still promising.

Recommendations for Carbon Nanotubes

- Develop solutions to lower the Schottky barriers at source/drain
- Develop solutions to remove the metallic CNTs
  Develop faster growing process
- Develop circuit design strategies to deal with variability induced by m-CNTs and doping fluctuation
- Develop compact models and design tools and evaluate the power-performance on real design contexts taking into account the physics of the device (quantum capacitance) and its parasitics.

Definition of FoMs or planned evolution

FoM / Planned Evolution
Too early stage technology to plan FoMs evolution, The FoMs of Silicon MOSFETs (Ion, Ioff, gm, SS) apply. Percentage of failure and variability due the metallic CNTs and bad orientation (failed growth)

Other issues & challenges, interaction with other areas

- II.3, II.4 and II.5 functional diversification
- II.6 heterogeneous integration

Medium Term [+5 years] ●●●●●+

Long Term [+10 years] ●●●●●●+●●●●●●

Key research questions/issues

- Metallic CNTs: CNTs are grown by a catalytic process that lead to semiconductor CNTs but also metallic CNTs. These metallic CNTs create shorts and hence transistor failure.
- Although the intrinsic device has extremely high mobility, the intrinsic performance is hindered by the source/drain access, composed of quantum resistance (mismatch in number of states in CNT compared to electrodes), Schottky barriers at the metal/nanotube interface, and parasitics series resistance.
- Schottky barriers in a CNTFET is the main issue for performance, impacting the characteristics not only the 'on' state (similar to a series resistance), but also the 'off' state, degrading the efficiency of the gate to switch off the channel, hence the leakage current and the subthreshold slope.
- In a thin gate oxide CNTFET, both Schottky barriers can become thin enough to allow the injection of both carriers simultaneously, leading to undesired ambipolar behavior.
- Although the quantum capacitance is extremely low, the coupling capacitance between the CNT and the surrounding conductors become more and more important at scaled dimensions and could hinder the benefit of the low intrinsic capacitance.

Application needs & Impact for Europe

- Nanotubes offer theoretically the potential of very fast (THz) and ultimately scaled transistors for logic applications, with self-assembly based fabrication. The issues of the Schottky barriers and variability caused by metallic CNTs are however at the moment show stoppers. The fabrication process might be cheaper but is slower, which is also an issue.
- CNTs are potential candidates for future via and wire material in nano-scale VLSI circuits, eliminating electromigration reliability concerns as they can stand much higher current density than copper interconnects.
- Transistors with properly functionalized CNTs are already being used as sensitive and selective chemical and biosensors.
- CNT-based nano-light sources and detectors may allow intra-chip optical communications and individual molecule level spectroscopy. Further integration to include optics could lead to a unified electronic-optoelectronic technology.

Technology and design challenges

- Technology solutions have to be found to remove metallic CNTs, or logic circuit design solutions to deal with caused variability and failure.
- Contacts: size-independent contact schemes with low Schottky barrier heights have to be developed that do not hinder the intrinsic benefit of the CNT transport.
- Solutions have to be found to screen the impact of the Schottky barrier on leakage. A solution is to use independent gates near source/drain and in the channel, but this will hinder gate scaling.
- Fabrication speed: non metallic catalysts are slow, metallic catalyst lead to possible metallic CNTs hence shorts and device variability.
- The growth direction of SWNTs on SiO_2-Si substrates is difficult to control since SiO_2 is an amorphous material. Misaligned CNTs lead to variability and failure.
- Non CMOS compatible metals like Au, Ti, Pd and Al are used for the source and drain electrodes and should be replaced by CMOS compatible options.
- High variability due to doping fluctuation in the ultra-thin body if n/p devices are made by doping (non ambipolar device).

Memories

The stand-alone market is currently dominated and driven by 3D NAND-Flash. This seems to be the main path on the roadmap for the next >5 years, with very limited global actors sharing market quotas (Samsung and Intel/Micron). It is more fruitful to focus on emerging non-volatile memories (eNVM) that can become the next product for specific applications, ie SCM/Storage Class Memory and embedded memories for IoT, automotive, low power markets. Also neuromorphic applications are seen as promising on a longer time scale as new potential applications are arising.
ENVM are substantially represented by the non-charge based technologies, PCRAM, OxRAM, CBRAM, MRAM and FeFET.

All these concepts struggle today to show a convincing potential for a product. The issues are quite similar for all of them, and can be summarized into three points: variability, retention at temperature and density. Various proofs of concept have been shown for each of those, and even a few products:

PCM (all standalone/storage class markets):

- SAMSUNG 64 MB, 65 nm (2010)
- Micron 128 MB, 45 nm (2011)
- Intel 32 GB, (2017)

RRAM (OxRAM and CBRAM)(consumer embedded):

- PANASONIC 64 KB, 180 nm (2013)
- Adesto 64 KB, 130 nm (2010)

STT-MRAM(all standalone market):

- Everspin 8 MB, 90 nm (2014)
- Avalanche Technologies 4 Mb – 8 Mb (2016)

From a European perspective the stand-alone market looks far away and running at an increasing pace. Embedded market seems to be the only field where a fair competition is still possible. Automotive-driven applications and non-mainstream technologies as FD-SOI can create the substrate where emerging eNVM can grow.

Currently the need for new memory concepts is clear and strong, driving considerable efforts into research. Emerging eNVM however are far from being ready, and the amount of new concepts can lead to a risky energy-dispersive research work.

In the short-time horizon, the main view needs to focus on clarifying which technology has most potentials for success. It can be agreed that each eNVM needs to be refined with respect to given specification, but it is also clear that, for the time being, the lack of specifications is not the development bottleneck. Rather, emerging technologies are struggling to match in a strong and reliable way any specification. As the need for scalable embedded memory is quickly rising (nodes <=28 nm) within 5 years we must expect to see a reliable demonstrator. Intel 3DXpoint technology, based on emerging NVM, suited for SCM application is probably the closest concept, but in the eNVM horizon no product exists that can claim this role.

We focus on two main aspects. First to describe the market needs and the actual situation and secondly to present the actual candidates that are most likely to contend the role of next eNVM. Summarizing in short the many aspects that characterize the NVM is not an easy task, but that indeed reflex the complexity of the NVM technology segment. We will discuss 5 different concepts that are currently challenging in the research effort to provide enough specs for convincing the market. Surely the application is there!

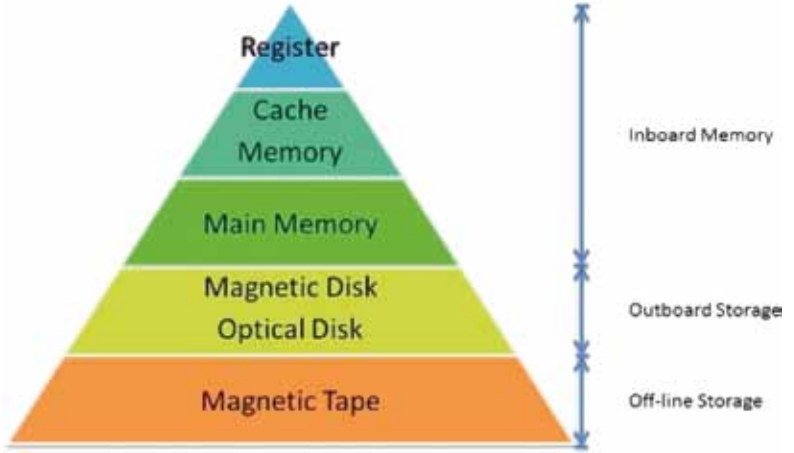


Fig. II.1.4: Different types of Memories

Memories, Concept 1 - OxRAM

Key research questions/issues

- HRS distribution reduction
- Operation energy reduction
- Forming Voltage reduction

Medium Term [+5 years]

- Much research efforts already spent with average results. In 5 years OxRAM must convince or will die:
- Cell shrinkage and/or encapsulation techniques can be beneficial to control variability and need to be investigated. It looks hard to find new materials after extensive research, but dopants and material phases are still an open topic.

Long Term [+10 years]

- HRS distributions tightly controlled. This can happen in 2 ways: 1. On known materials like HfO_2, working on scaling, encapsulation, programming techniques, CF confinement; or 2. Changing material. This way seems less likely, because HRS spread looks to be intrinsic in the CF-like switching. At this horizon market must see more than a convincing production a niche market, some volume must be expected.

Application needs & Impact for Europe

Medium Term [+5 years]

- Embedded memory or storage class memory. Need in automotive, µC for general purpose, consumer market, …

Other issues and challenges, interaction with other areas

Medium Term [+5 years]

- Need to confine CF. work on the cell encapsulation and interfaces.
- New designs on system level can open new (niche) market. Ex: IoT (this can be a mainstream), neuromorphic, TCAM, NV-DRAM, memory computation…
- However, crossbar will be necessary for density, need for BEOL access diode

Recommendations for OxRAM

HRS broadening is the Challenge. New materials, new programming schemes need to be investigated.

Definition of FoMs or planned evolution

FoM / Planned Evolution	2023	2033
BER	BER<1E-6 (w/0 ECC)	BER<1E-6 (w/0 ECC)
Endurance	>1E5	>1E6 (for SCM >1E10)
Retention	10Y@85C and soldering reflow compliant	10Y@85C and soldering reflow compliant
Forming voltage	<3 V	<2 V

Memories, Concept 2 - CBRAM

Key research questions/issues

- HRS distribution reduction
- Endurance increase
- Improve data retention

Medium Term [+5 years]

- Specimens are on the market! New generation required and attended. Can CBRAM meet specs for SCM?

Long Term [+10 years]

- CBRAM has to improve data retention, to meet Flash standards (85C 10y) or 125C 10y for automotive. Endurance is less stringent for most applications, but 1E5 will be required.

Application needs & Impact for Europe

- Embedded: integration at scaled node <28 nm. Scaled SoC, automotive application (but spec need to be demonstrated). IoT, Security applications (embedded security)
- SCM:
- Applications on PC, tablet, phones, consumer markets, High speed computation (Fast boot), Recovery after power loss
- Computing in memory

Other issues & challenges, interaction with other areas

- Need to confine CF. work on the cell encapsulation and interfaces.
- New designs on system level can open new (niche) market. Ex: IoT (this can be a mainstream), neuromorphic, TCAM, NV-DRAM, memory computation…
- However, crossbar will be necessary for density, need for BEOL access diode

Medium Term [+5 years]

- Difficult to say, CBRAM and OxRAM have big challenges in the 5 years horizon already

Recommendations for CBRAM

Same as OxRAM plus a special focus on data retention, which is probably the most challenging topic for CBRAM. Since CBRAM are already available as sampling parts, the identification of applications and assessment of REAL specs is mandatory in the next few years.
This technology exists in Europe (Altis) and need to be evaluated.

Definition of FoMs or planned evolution

FoM / Planned Evolution	2023	2033
BER	BER<1E-6 (w/0 ECC)	BER<1E-6 (w/0 ECC)
Endurance	>1E5	>1E6 (for SCM >1E10)
Retention	10Y@85C and soldering reflow compliant	10Y@85C and soldering reflow compliant
Forming voltage	<3 V	<2 V

Memories, Concept 3 - PCM

Key research questions/issues

- Improve data retention
- Confine material for energy reduction

Medium Term [+5 years]

- Specimens are on the market! New generation required and attended. Probably the most mature option. Need to be tested by customers.

Long Term [+10 years]

- Scaling can be a great challenge. Research needs to be focused in that direction.

Application needs & Impact for Europe

Medium Term [+5 years]

- Embedded: integration at scaled node <28 nm. Scaled SoC, automotive application (but spec need to be demonstrated). IoT, Security applications (embedded security)
- SCM
- Applications on PC, tablet, phones, consumer markets, High speed computation (Fast boot), Recovery after power loss
- Computing in memory

Other issues & challenges, interaction with other areas

Medium Term [+5 years]

- Need for cell thermal confinement GST etching required. 2 research axes: 1. Materials improvement for quicker write/erase and 2. Improvement for higher thermal stability (for embedded applications, 150 C automotive + 260 C 2' for soldering reflow)

Long Term [+10 years]

- Scalability at 1x nodes with thermal confinement looks as a main challenge.

Recommendations for PCM

PCR is probably the most mature eNVM solution. Some specimens exist on market (see above), however customers are skeptical. This is probably due to a very conservative approach in the memory market, which is historically very prudent. This could then represent a potential for European industry, which could differentiate itself, investing more on PCR development.

PCM needs to progress on integration, necessary for GST patterning. In addition, material research needs to be continued to optimize data retention for scaled nodes. Demonstrating the possibility to scale PCM cell to nodes <<28 is mandatory, and possible axis research exist already (e.g. confined cells).

Definition of FoMs or planned evolution

FoM / Planned Evolution	2023	2033
BER	BER<1E-6 (w/0 ECC)	BER<1E-6 (w/0 ECC)
Endurance	>1E5	>1E6 (for SCM >1E10)
Retention	10Y@85C and soldering reflow compliant	10Y@85C and soldering reflow compliant
Forming voltage	<3 V	<2 V

Memories, Concept 4 - MRAM

Key research questions/issues

- integration
- consumption
- scaling

Medium Term [+5 years]

- Process is still a challenge due to etching of complex stacks. Scalability is also challenging. Need to work on design to reduce consumption and currents.

Long Term [+10 years]

- Below 14 nm, a new cell structure is required. Increasing the number of interfaces to stabilize the magnetic polarization.

Application needs & Impact for Europe

Medium Term [+5 years]

- Embedded: integration at scaled node <28 nm. Scaled SoC, automotive application (but spec need to be demonstrated). IoT, Security applications (embedded security)
- SCM: Applications on PC, tablet, phones, consumer markets, High speed computation (Fast boot), Recovery after power loss
- Computing in memory

Other issues & challenges, interaction with other areas

Medium Term [+5 years]

- Main issues related to integration and COST. Some samples are available (mainly Everspin). Fab integration demonstration required. New tools required for integration (large Capex). Need to demonstrate enough magnetic immunity, reduce programming and reading currents by a factor 5-10. Products expected in 1-2y horizon!

Long Term [+10 years]

- Integration of MRAM process in foundries needs to be assessed. Reduction of programming current required (10-100 pJ/bit can be a reasonable figure).

Recommendations for MRAM

MRAM are becoming extremely popular in these years. However, etching, thus integration, problems can be much harder to solve than expected. Plus, the high current consumption can be a serious drawback for real applications, in particular for IoT.

Definition of FoMs or planned evolution

FoM / Planned Evolution	2023	2033
BER	BER<1E-6 (w/0 ECC)	BER<1E-6 (w/0 ECC)
Endurance	>1E5	>1E6 (for SCM >1E10)
Retention	10Y@85C and soldering reflow compliant	10Y@85C and soldering reflow compliant
Forming voltage	<3 V	<2 V

Memories, Concept 5 - FeFET

Key research questions/issues

- Increase of ΔV_{th}
- Variability control
- Physics understanding

Medium Term [+5 years]

- Mostly for embedded application at scaled node. Only one main actor (GF and Namlab)
- First proof of concept available. At 5 years a commercial generation is required. Research on HfO_2 dopant needed to increase coercive field ΔV_{th} shift

Long Term [+10 years]

- Difficult to establish: FeFET is a very recent device.

Application needs & Impact for Europe

Medium Term [+5 years]

- Embedded: integration at scaled node <28 nm. Scaled SoC, automotive application (but spec need to be demonstrated). IoT, Security applications (embedded security)
- SCM: Applications on PC, tablet, phones, consumer markets, High speed computation (Fast boot), Recovery after power loss
- Computing in memory

Long Term [+10 years]

- FeFET, if succesfull can be a real groundbraking technology, since it can truly be integrated along with logic gates. However this will be only ensured in the long term horizon

Other issues & challenges, interaction with other areas

- Still in a very early stage. In 5 years, needs to find golden material, demonstrate data retention and endurance. Main challenges: increase memory window and data retention. Also disturb immunity looks an issue to be addressed.

Competitive situation of FeFET

Non-charged-based Memories (PCRAM, MRAM, RRAM/OxRAM & CBRAM; FeFET) can potentially overcome many technology limitations of traditional charge-based memories and could be used for many applications (e.g. Embedded and SCM/Storage Class Memories).

Recommendations for FeFET

Widen the material screening in addition to the standard $Si:HfO_2$. A lot of work is necessary on the interface between channel and Fe layer.

Definition of FoMs or planned evolution

FoM / Planned Evolution	2023	2033
BER	BER<1E-6 (w/0 ECC)	BER<1E-6 (w/0 ECC)
Endurance	>1E5	>1E6 (for SCM >1E10)
Retention	10Y@85C and soldering reflow compliant	10Y@85C and soldering reflow compliant
Forming voltage	<3 V	<2 V

3D sequential integration

3D sequential integration is an alternative to conventional device scaling. Compared to TSV-based 3D ICs, 3D sequential process flow offers the possibility to stack devices with a lithographic alignment precision (few nm) enabling via density > 100 million/mm^2 between transistors tiers (for 14 nm design rules). It's also possible to merge several technologies and materials. The typical structure is shown in Fig. II.1.5.

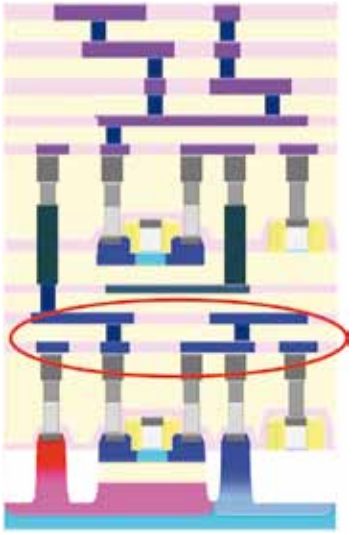
Competitive situation of 3D sequential integration

3D sequential integration is a very interesting approach for the following developments: CMOS-on CMOS for area scaling, Imagers co-integrated with Logic, Computation immersed in memory, Sensors on CMOS for IoT, Beyond CMOS devices co-integration w/ CMOS.

Recommendations for 3D sequential integration

- To define which applications will benefit from very high density interconnections (IOT, neuromorphic…)
- Development of a 3D place and route tool
- 3D sequential can combine any CMOS from bulk planar to Finfet or FD-SOI…
- FD-SOI and 3D integration can respond to future neuromorphic and quantum computing approaches

Top tier



Bottom tier

Fig. II.1.5: 3D sequential integration of various devices

3D sequential integration

Other issues & challenges, interaction with other areas

- Link with II.8: enabler for neuromorphic computing/ quantum computing
- Link with II.3: sensors+ CMOS co-integration enabler
- Link with II.6: need for understanding system level benefit of 3D sequential options
- Link with II.7: development of low resistance, thermally stable BEOL materials; low T processes: wafer bonding, epi, gate stack materials/interfaces development for low T.

Key research questions/issues	*Medium Term [+5 years]*	*Long Term [+10 years]*
• Which application will benefit from very high density interconnections?	• For IoT: intelligent local processing of the data to decrease the bandwith of data transmission. • Neuromorphic architectures	
• How to enable ultra-fine grain interconnections between layers?	• CoolCube and sequential integration	• Active 3D interconnection (programmable), DNA based interconnection for ultra-high density non bi-directionnal interconnection (to enable more close neighbours)
• Thermally stable metallization, with low resistance	• Interconnect metallization materials and associated diffusion barrier materials which provide low resistance and required stability throughout the temperature bonding cycles.	• Co, silicided intercos
• Reliability for low T gate stacks	• Reliability in low temperature gate last integration	
• Low thermal cycle device performance	• Full low temperature CMOS transistors @ 500 °C with good gate stack reliability	
• Test methodology	• For top and bottom characterization	

Application needs & Impact for Europe	*Medium Term [+5 years]*	*Long Term [+10 years]*
• CMOS-on CMOS for area scaling	• SRAM memory block to block	• Enabler for in memory computing architecture and neuromorphic
• Imagers co-integrated with Logic	• 3D pixels for smart pixels (digital computing won't be at the local scale) • Local memory storing	• Smart pixels with local computing capabilities (each pixel will benefit from its local computing unit)
• Computation immersed in memory		
• Sensors on CMOS for IOT	• NEMS, bolometers with the local analog parts with better performance than ASIC and better cost than co-integration	• Multisensing platform
• Beyond CMOS devices co-integration w/ CMOS	• TFET, 2D TMDs, graphene	• Qubit addressing

Technology and design challenges	*Medium Term [+5 years]*	*Long Term [+10 years]*
• Design tools optimized for Sequential 3D not available	• Use of 2D existing tools to provide partially optimized (fold or shrunk techniques) 3D place and route tools.	• Actual 3D place and route tools with 3D optimization at the logic gate scale.
• Reducing parasitics in each implementation	• Wire length decrease	• Material optimization
• Thermal management/selfheating mitigation	• Layout optimization	• Layout + heat spreaders + thermoelectric cooling, energy harvesters, new interconnection materials
• Manufacturing challenges as in a) above	• Same performance, same yield as 2D integration	• Yield on multi-Tiers

Definition of FoMs or planned evolution

FoM / Planned Evolution	Medi term: 5+	Lang term: 10+
Top level device performance and reliability	Similar to 2D	
Contamination management	In industrial fab with W or Cu interconnect	
System level performance vs 2D or 3DTSV	Same as 2D, or 3DTSV	> than 2D, or 3DTSV
System level area vs. 2D or 3DTSV	Same as 2D, or 3DTSV	< than 2D, or 3DTSV
System level cost comparison vs. 2D or 3DTSV including yield	Same as 2D, or 3DTSV	< than 2D, or 3DTSV
Multi-tier stacking	Same as 2D, or 3DTSV	More than 2 tiers

Modelling/Simulations Tools

Modelling and Simulation tools are needed for the proof of concept of new devices, benchmarking and screening of technology options, and assessment up to circuit level (DTCO). They are also very important in order to assist interpretation of experimental data and extraction of the physically meaningful parameters. They should be predictive of trends and give actual absolute average values and variability.

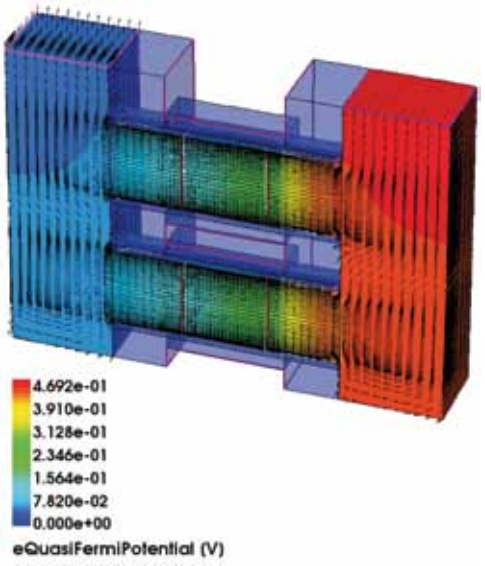


Fig. II.1.6: Simulation of electron quasi-Fermi potential and the current vector in a FinFET

Key research questions/issues	*Medium Term [+5 years]*	*Long Term [+10 years]*
• Modelling full band structure of confined (2D, 1D) materials of interest to enable electrostatics and transport studies	• DFT, TB, KP, EPM methods and related NP-EMA parameterizations of most promising materials • quantum electrostatics models in 2.5D and 3D	• DFT, TB, KP, EPM methods and related NP-EMA parameterizations of most promising materials • For winning solutions
• Models suited to steer the selection of device architectures and of channel materials (FD-SOI, FinFET, UTBB DG, GAA, NW, NSH, stacked NW, …) + Static performance (I_{on}, I_{off}, SS, DIBL, V_T, gm, Avi, …) + Dynamic performance (Cij, Tsw, τFO4, f_T, f_{max}, …)	• Multi-valley Multi Sub-band models of layered structures including wave-function penetration • Semi-classical and quantum transport coupled electro-thermal models (including all relevant scattering mechanisms) • Almost arbitrary geometry, material (sSixGe(1-x), GeSn, III-V), orientation and strain combinations	• Extension to transient time-dependent and time-harmonic small signal solutions • Inclusion in TCAD
• Models of novel steep-slope device concepts for ULP electronics integrating new materials and suited for the selection of most promising options + Attention to leakage phenomena	• Heterojunction tunnel FETs • Ferro- and Piezo FETs • 2D materials FETs • Calibration to experiments	• For most promising solutions • Non-ideal effects (traps, etc.) • Extension to transient time-dependent and time-harmonic small signal solutions • Inclusion in TCAD
• Models for 3D vertical transistor stacking and related parasitics (resistances and capacitances)	• Multiscale approaches combining accurate physical description of the channel and access regions with large scale DD models for parasitics (change of carrier gas dimensionality, ultra-small contacts, etc.)	• Progress toward full atomistic descriptions of nanoscale devices (DFT, TB, etc.)
• Simulation of variability, fluctuations, impact of traps and defects in nanoscale devices in Silicon and in new channel/dielectric materials	• Atomistic descriptions of gate dielectrics, interfaces, barriers, defects, traps, surfaces and link to continuum models for selected devices/materials • Statistical models for most promising devices	
• Reliability modeling in new material systems (HCI, BTI, …)	• Identification of degradation mechanisms and degradation models	• Implementation of degradation models in design tools
• Process modeling for new materials, support to DTCO	• Requirements will be application specific	• Requirements will be application specific

Application needs & Impact for Europe	*Medium Term [+5 years]*	*Long Term [+10 years]*
• Accelerate development and strengthen competitive advantage in the field of ULP technologies	• …	• …
• Modeling and simulation SMEs in Europe form a small but healthy ecosystem (GSS, GlobalTCAD, TiberTCAD, NextNano, Quantavis, QuantumWise, MDlab, etc.)	• Potential for further growth (atomistic, multiscale, reliability, …)	• Consolidation of the M&S SME sector ?
• "Modeling Technology" transfer from academia to industry • Knowledge transfer to large research laboratories and industry	• Integration of advanced research tools in general purpose TCAD platforms	• Ability to attract bright minds to the field of nanoelectronics M&S • Ability to maintain high quality education in applied math and physics subjects

Technology and design challenges

- Model verification and experimental calibration at different levels of physical detail

Competitive situation of Modelling/Simulations Tools

The modelling and simulation tools are of fundamental interest in order to speed-up technological optimization and reduce the cost of technology development. European teams have a very strong expertise in this field.

Recommendations for Modelling/Simulations Tools

- Promote dedicated M&S projects in application areas of interest for the European nanoelectronics community (ULP electronics, power devices, nano-bio sensing, neuromorphic memory, quantum computing, etc…)
- Identify M&S needs well in advance, systematically devote adequate share of resources, also by embedding modeling in all technology projects
- Privilege approaches that account for arbitrary geometry and all relevant physics, e.g. multi-scale, valley, subband, electrostatics of layered structures with wavefunction penetration, transport models comprehensive of tunneling and all relevant scattering mechanisms (remote-X, SR).

Definition of FoMs or planned evolution

FoM / Planned Evolution	Medi term: 5+	Lang term: 10+
Physical device dimensions and computational dimensionality of manageable problems (e.g.: length, cross section, volume, no. of materials, regions, atoms, number of eigenstates, number of particles, wall clock time, CPU time)	Steadily getting better because of improvements in computing resources and efficiency of simulation methods	Steadily getting better because of improvements in computing resources and efficiency of simulation methods
Ability to incorporate all relevant physics	FoMs will be technology dependent	FoMs will be technology dependent
Ability to achieve the degree of accuracy required by applications (device design, benchmarking of technologies, etc.)	FoMs will depend on degree of technology maturity, application and type of device	FoMs will depend on degree of technology maturity, application and type of device
Computational resources accessible to academic, research institute and industrial environments	Improved because of evolution in conventional computing technology and related costs	Distributed scientific computation?

Other issues & challenges, interaction with other areas

	Medium Term [+5 years] ●●●●●+	*Long Term [+10 years]* ●●●●●●+
• Memory modelling	• …	• …
• Automotive and Energy: Verified and calibrated models down to TCAD level for large bandgap materials (e.g. SiC, GaN, etc.)	• TCAD compact models for material properties and physical processes	• Widespread use of TCAD in design of electron devices for the applications
• Sensors: dependable simulation of analyte diffusion and transduction processes including statistical aspects	• Solid/liquid electrolyte materials and interface models available in multiscale-multiphysics and TCAD simulation tools • Coupled analyte diffusion / transport modeling	• Models for functionalization layers responsible of selectivity • Models for analytes • Broader usage of commercial and ad-hoc simulation tools of transduction processes • Achieve simulations “predictive” of trends observed in actual devices and suited to interpret the measured statistics

Characterization Tools

CMOS technologies evolve from bulk to FD-SOI/FinFET and Nanowires due to improved electrostatic control, better scalability and lower variability, but increasing issues of transport and interfaces in Ultrathin Bodies and new materials. Therefore, reliable characterization methods have to be developed for the next generation of nanoscale devices as shown in Fig. II.1.7.

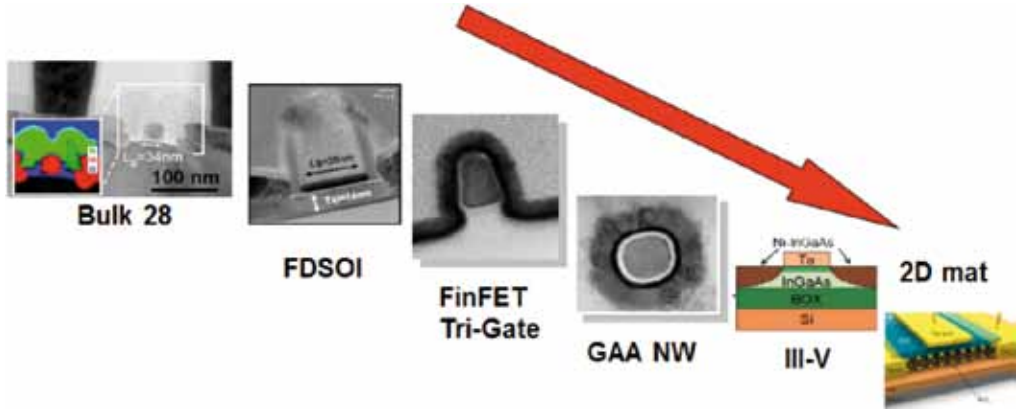


Fig. II.1.7: Evolution of Transistor architectures and Channel materials for ultimate MOSFET integration

Competitive situation of Characterization Tools

The characterization tools are of fundamental interests for technological optimization. European labs have a very strong expertise in this field.

Recommendations for Characterization Tools

- CV/capacitance-voltage measurements are still feasible but specific test structures are needed (multi fingers or RFCV) on FD-SOI, FinFET, Nanowires…
- MOSFET parameter extraction requires the development of new methods and on new 2D materials, III-V, Ge,…
- The source-drain resistance Rsd is a key parameter
- Mobility and transport parameters are measurable on standard MOSFETs down to very small Lg but the magneto-resistance is very useful and should be developed
- Traps and interface quality can be assessed even on very small area devices and methods using LFN/low frequency noise or RTN/random telegraph noise are becoming very useful (C-V, CP/charge pumping are area limited unless multi finger is used)
- Stochastic Variability becomes critical and must be measured in static and in dynamic modes => problems for non mature technologies but also for TFET, FeFET

1 star = little importance
2 stars = medium importance
3 stars = high importance

Medium Term [+5 years]

Long Term [+10 years]

Key Challenges in Electrical Characterization

Nanowires

- Specific test structures with multifingers necessary for increase device area especially for vertical NW with short channel features.
- In III-V gate stack, issue with border trap characterization by CV & Gw techniques on large area, LF noise proves efficient even on small area devices…
- III-V channel transport properties: Hall effect test structure for free carrier density assessment vs total carrier density from CV data, Hall mobility vs effective mobility, low temperature studies for scattering mechanisms identification…
- Similar methods should apply to 2D materials with critical issues on interface (LF noise, CV & Gw techniques, current DLTS, Fast IV for hysteresis analysis…). Any specificity for 2D materials should be pointed out.

FD-SOI/FinFET

- For electrical characterization, it should be mentioned that most of existing I-V and C-V measurement tools have good enough resolution and accuracy for DC and low frequency range. RF test equipment currently available in industrial and academic labs are also of sufficient accuracy up to 100 GHz frequencies for S parameter measurements and subsequent data de-embedding exploitation.
- Stack parameter extraction and associated wafer scale variation: Challenge due to multiple layers combining front gate dielectric, channel, BOX and ground plane, assessment of work function for front and back gates, discriminate charge and dipole contribution in front HK dielectric, Solutions: confront TCAD simulation results and statistical CV data on large area MOSFET at wafer scale, use of specific CV test structures with variable EOT over wafer (beveled HK thickness)…
- Ferrolectric and negative capacitance MOSFET: challenge in polarisation assessment using specific test structure (conducting layer in between Cox and Cfe capacitance, cf Rusu 2012) or using standard Sawyer-Tower circuit providing polarization vs field characteristics, associated strain measurements should be desirable for piezo-Ferro materials…
- Transport properties (mobility, velocity) and parameter extraction in channel of nano MOSFETs: Challenge due to parameter extraction (channel vs access), finding scattering mechanisms and ballistic contribution, solution by RF split CV, magnetoresistance measurements, low temperature characterization…Improved parameter extraction are needed for Rsd assessment, especially if they depend on gate voltage (Rtot vs L method, Y function method, dR_{tot}/dL method…). Need for appropriate parameter extraction methods adapted to low voltage operation with V_{dd} close to threshold voltage (V_{dd}<0.4 V). Confrontation to TCAD simulation results will also be worthwhile for validating extraction methodologies.
- Intrinsic and parasitic Capacitances of nano MOSFETs: Challenge due to small capacitance values, solutions: use of multifinger MOSFET structures, use of RF CV technique based on S parameter measurements…
- Strain/stress in nano MOSFETs: Challenge due to nanoscale probing along the channel for correlation to mobility enhancement using holographic TEM, HRTEM, NBED, PED, CBED techniques…
- Interface quality and reliability related to initial and stress induced traps: Challenge due to small area of nano MOSFETs, device-to-device stochastic variations, solutions: use of multifinger MOSFET structures, use of dedicated techniques applicable to small area such as LF noise, AC transconductance, drain current DLTS,… requirement for statistical measurements…
- Variability in nano MOSFETs: Challenge due to requirement for statistical measurements, discrimination of local vs global variability sources, time dependent instability and dynamic variability measurements at µs to ns time scale, solutions: use of specific methodologies based on DC drain current variance analysis vs bias, use of addressable array structures for enhanced statistics, use of ultra-fast I-V measurements with specific test structures …
- Self-heating effect (SHE): Challenge due to self-heating arising from BOX, need for test structures for measuring channel temperature, discrimination of SHE impact on reliability…

TFET

- Proper parameter extraction methodology needed due to special BBT operation, assessment of local drain current variability needed, impact of interface quality and junction doping/gap profile on BBT, correlation to physical characterization….
- A special attention should be paid to determine whether carrier injection on either side of the device occurs via band-to-band tunnelling or single carrier tunnelling through a Schottky barrier. This can be achieved by analysing the I_d-V_d output characteristics under forward and reverse operation.
- Better assessment of trap assisted tunnelling in TFET operation.

FinFET

- Idem FD-SOI with specific multifinger test structure needed.

Memories

- Specific challenges in characterization: ultra-fast tool for programming and reading, LF noise and RTN, cycle-to-cycle and device-to-device variability, physical characterization of filamentary nature by local AFM probe for OXRAM/CBRAM, data retention after thermal acceleration test for emerging memories…

3D sequential integration

- Idem FD-SOI with also Specific challenges in characterization: differentiate top vs bottom layer devices in terms of transport, interface and variability properties

Reliability

Ensuring device operation within specified margins for the entire expected lifetime of the application is a crucial aspect of novel device design. Device reliability is therefore a key figure of merit (FoM), together with Power, Performance, Area, and Cost. Device reliability can be optimized during the novel device design stage if the underlying degradation mechanisms are well understood and can be traded for the other key FoMs. Deep, physics-based understanding of the degradation mechanisms allows determining the real Safe Operating Area (SOA) of the device.

Subsequently this knowledge can be leveraged during design of both logic and memory applications employing devices based on existing as well as novel materials and architectures. The gate-oxide-related device degradation mechanisms include Random Telegraph Noise (RTN), Bias Temperature Instability (BTI), Hot Carrier Degradation (HCD), and Time-Dependent Dielectric Breakdown (TDDB). Since deeply scaled devices with gate areas of 102 – 103 nm^2 will contain only a handful of defects in their gate oxide, the degradation mechanisms are best described and mitigated if the properties of individual oxide defects are well understood at the atomic level. The individual oxide defect properties include their capture/emission and/or generation rates and their voltage (or electric field) and temperature dependences, and the impact of defects on the device characteristics. This in turn enables prediction of not only the mean degradation, but also the statistical distributions of degradation in a population of devices, i.e., time-dependent variability. The mean and variability degradation-enabled models can be propagated through compact models to higher design abstraction levels.

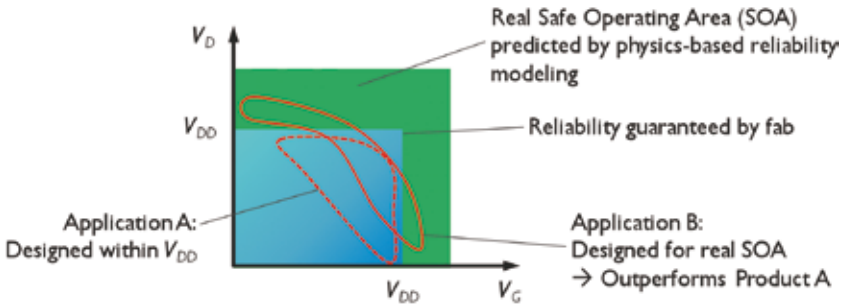


Fig. II.1.8: Illustration of benefit of designing for real Safe Operating Area

Key research questions/issues	*Medium Term [+5 years]*	*Long Term [+10 years]*
• Physical properties of gate oxide defects responsible for the main degradation mechanisms in existing and novel material systems	• Experimental extraction • First-principles DFT modeling • Development of models including • Preexisting defect capture/emission rates and their voltage (or electric field) and temperature dependences • Defect generation rates and their voltage (or electric field) and temperature dependences • Implementation of models in TCAD tools	• Implementation of models in TCAD tools
• Impact of gate oxide defects on characteristics of existing and novel architecture devices	• Experimental extraction • TCAD modeling and verification • Implementation of models in TCAD tools	• Implementation of models in TCAD tools
• Device carrier transport and energy distribution modeling	• Incorporation of relevant scattering mechanisms • Incorporation of quantum mechanical effects • Interaction of carriers with defects • Implementation of models in TCAD tools	• Implementation of models in TCAD tools
• Temperature profiles inside devices	• Development and measurements of dedicated test structures	• Implementation of models in TCAD tools
• Development of reliability-enabled compact models	• Coupling of charge and heat carriers for realistic temperature profiles • Efficient reduction of mean and statistical defect properties into closed-form formulas	• Acceptance and standardization of methodologies by the semiconductor industry

Application needs & Impact for Europe

- Leveraging the full potential of the devices during application design
- Development of methodologies to propagate defect properties to lifetime projections and SOA determination
- Acceptance and standardization of methodologies by the semiconductor industry

Technology and design challenges

• Experimental extraction of statistically significant defect properties	• Development of methodologies for large scale technology data harvesting, including dedicated (on-chip) circuits • Improvements in efficiency and refactoring of reliability models • Computational improvements	• Acceptance and standardization by the semiconductor industry
• Computational complexity of reliability enabled TCAD		
• Development of reliability-enabled compact models	• Efficient incorporation of mean and statistical defect properties	

Reliability

Definition of FoMs or planned evolution

FoM / Planned Evolution	Medi term: 5+	Lang term: 10+
Full reliability models accurately reproducing mean shifts and distributions in main device parameters, including $V_{th,SS}$, g_m, I_{on}, in V_G and V_D and temperature accelerated testing	Model prediction within 20% of accelerated tests experimental data	Model prediction within 10% of accelerated tests experimental data
Reliability-enabled compact models accurately reproducing mean shifts and distributions in main device parameters, including $V_{th,SS}$, g_m, I_{on}, in V_G and V_D and temperature accelerated testing		Model prediction within 20% of accelerated tests experimental data
Computationally manageable reliability-enabled TCAD models	1 IV characteristic per degradation condition calculated in 1 real-time hour	100 IV characteristics per degradation condition calculated in 1 real-time hour

Other issues & challenges, interaction with other areas

- Concepts “Modelling/Simulations Tools” and “Characterization Tools”

Competitive situation of Reliability

Physics-based reliability models enable determination of the real SOA of novel devices and thus leveraging the full potential of the devices during application design and optimizing application reliability with other key FoMs. This know-how will allow European entities to retain a competitive advantage and offer it to the entire semiconductor industry.

Recommendations for Reliability

- Consistently include reliability as a key FoM during novel device design and down-selection
- Dedicate adequate resources to reliability parameter extraction, modeling, and testing in both existing and new material systems
- Promote projects dedicated to reliability enabling collaboration of a broad spectrum of expertise, including physicists, material scientists, technologists, TCAD engineers, and designers
- Develop methodology to propagate reliability to higher application design abstraction layers

Synergies with other topics

Important links of Advanced Logic/Memories with II.3-8.

Recommendations for Nanoscale FET

In the More Moore field, there are also strong interests in Europe for specific activities dealing with very low power systems, leading to possible disruptive applications for instance for future IoT systems, for embedded memories, for 3D sequential integration, or for application driven performance, e.g. high temperature operation for the automotive industry using for instance FD-SOI.

- For Nanowires, which are very interesting for very low power nanoscale devices and therefore important for the EU, identify the best material and geometry options for logics (high-speed as well as low-power), develop millimeter wave front-ends with III-V MOSFETs (applications for communication, radar), and consider the 3D aspects of processing
- For FD SOI, which is a strong advanced technology developed in industry and academia in the EU, develop differentiated options (RF, Embedded Memories, Imaging or molecules sensors) on FD-SOI (applications for automotive, IoT, smart sensors…), ULP design (V_d <0,4 V) for IoT market (wearable, medical…), and 3D integration for future neuromorphic and quantum computing approaches
- For FinFET, develop co-integration of different channel materials, low contact resistivity and high strain solutions, improve finFET analog performance
- For NCFET, identify the maximum switching speed, the optimal dimensions, develop thin Hafnium based Ferroelectric layers, investigate the scaling potential of the device
- For CNTFET, develop solutions to lower the Schottky barriers at source/drain, to remove the metallic CNTs, faster growing process, design strategies to deal with variability induced by m-CNTs and doping fluctuation
- For Memories, very important in the EU for embedded applications:
  - OxRAM, HRS broadening is the Challenge. New materials, new programming schemes need to be investigated
  - CBRAM, same as OxRAM plus a special focus on data retention, which is probably the most challenging topic for CBRAM
  - PCM, needs to progress on integration, necessary for GST patterning. In addition, material research needs to be continued to optimize data retention for scaled nodes
  - MRAM, etching, thus integration, problems can be much harder to solve than expected. The high current consumption can be a serious drawback for real applications, in particular for IoT
  - FeFET, widen the material screening in addition to the standard Si:HfO_2. A lot of work is necessary on the interface between channel and Fe layer.
- For 3D sequential integration, technology with important research activities in the EU, define which applications will benefit from very high density interconnections (IOT, neuromorphic…), and develop a 3D place and route tool
- For Modelling/Simulation, Characterization and Reliability, which are strong European domains, develop new tools taking into account all the new materials, technologies and device architectures in order speed-up technology optimization and reduce the cost of technology development. A particular attention should be given to the development of compact models and design tools for novel types of materials and devices.

II.2 Connectivity

Executive summary

The connectivity functions are everywhere to do the link between all other electronic functions. From the sensors and actuators to the processors and microcontrollers, from the sensor nodes to the gateways, from the gateways to the cells from the cells to the data centres, and all over the world. Inside each of these units, the connectivity links the computers to the memories, the core of multicores in High Performance Computing applications, and the peripheral devices to the central computing units.

The connectivity functions can be differentiated depending on the range and the nature. The nature of such function are wireless (in radio frequency mmW, THz bands, or visible light), or wireline (in copper or optical fiber). The range of such functions can be sorted out depending on the distance, the ultra-short range, is in the µm to cm distance; the short range is under 100 m, while the long range covers distances over 100 m.

The present biggest connectivity market field is dedicated to the data communications, especially for cellular (WAN), WLAN, WPAN, NFC, and incoming WSN and IoT communications. Then we can distinguish two other market fields, especially in Europe, even if they use, or are be connected to the first one: the automotive market which is at the beginning of the autonomous vehicle revolution, and the "health & security" market which will transform drastically our way of life in the next decades.

In the data communication field, we can distinguish three main families using the link distance criteria, the outdoor and cellular, as example 5G and future generations, the indoor communication mainly represented today by the WiFi links, and a not visible one, which can be called the In Devices one, or the communication between dies and packages in an equipment.

Relevance and Competitive value

If we look at the expectations on the technologies, the difference is mainly done by the different functions as Power Amplifiers, Low noise Amplifiers, Antennas in Wireless field, or Modulator Drivers, Laser Drivers, Trans Impedance Amplifiers, Modulator, Laser Diodes, and PIN diodes in Wireline field, we have to implement for the different transceivers. In this domain, the More Than More axes is privileged, (actives, NEMs and MEMs, and passives components), and the multi-physics assembly can bring advantages versus present solutions.

In counterpart, we can notice, that, whatever the transceivers are, we have common functions as the Phase Frequency generation, Local Oscillators in Wireless field, Phase Frequency Lock Loop and Clock Recovery in Wireline field. For these function the expectation is mainly the same whatever the selected communication link. In this domain, the More Than More axes is also privileged, (actives, NEMs and MEMs, and passives components). As previously, the multi-physics assembly can bring advantages versus present solutions.

Concerning the signal modulations and demodulations, the difference is mostly done by the design way, the functions are done in an analog approach or a digital one. Then, depending on the approach, the technology expectations are different. In an analog approach, the active More Than More axes is privileged, and, in a digital or "digital like" approach, the More Moore will bring the cost and the efficiency.

How to evaluate the Figure of Merit of a function?

This question is one of the main issue we face in Connectivity, as it is very difficult to compare wireless or wireline solutions. I would propose an approach, which is under discussion with NEREID experts: The industrial concern is to evaluate what is the efficiency of a function versus the cost of this function.

Starting from this ratio, we can try to define what the efficiency of a connectivity function is: The efficiency could be the data rate multiply by the range moderated by the error rate and divided by the power consumption. We can call this efficiency, the Technical Efficiency FOM.

And what is the cost of such function: The cost is very complex to estimate, as we don't have the information. It could be composed of the fabrication cost (initial cost), depending on the technology cost, the packaging cost and the test cost, and the exploitation cost. This will be called the Economic FOM.

The proposed formulae for the technical efficiency FOM is the following one:

FOM = Data_rate (Gbs, Mbs, Kbs) × Distance (m, km); depending on the specificities, Power consumption and BER can be added as challenges.

The cost is one important parameter, especially in consumer market, and the difficulty to have accurate information on it, will not allow experts to introduce

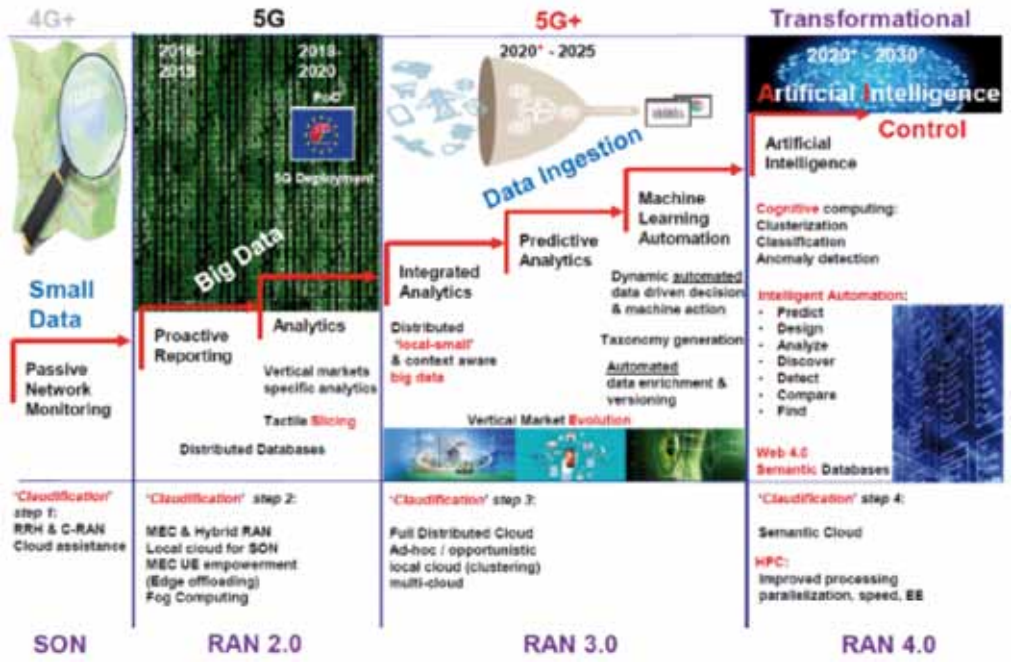


Fig. II.2.1: 5G and Beyond 5G Roadmap: From SON to RAN 4.0

it in the FOM. Depending on the application, it will be mentioned in the challenges.

Societal benefits

The connectivity functions will be everywhere in the connected world, from the physical world, (things and the persons, the autonomous objects, (factory 4.0, autonomous vehicles…), the Cyber Physical Systems), to the cloud, (E-Health, Intelligent Transport Systems, E-Security, E-Functions and computing…) in a big data concept; and from the cloud to the physical world.

Vision

The connectivity challenges are not limited to the physical quantities, but also to the privacy of exchange data, the security of a communication and the safety of the consequence of the exchanged data. We will try to explain in few sentences these different challenges:

- The Physical quantities for the next 5 years:
  - Traffic multiplied by 10 000
  - Energy per Bit divided by 1000
  - Capacity per area multiplied by 10 or connection density per Km² multiplied by 10
  - Mobility up to 500 km/h
  - Data Rate average per connection 100 Mbs
  - Data Rate peak per connection 10 Gbs
  - Latency less than 1 ms
  - Spectrum efficiency multiplied by 3
  - Connected devices multiplied by 100 (without IoT connection).
  - IoT connections more than 100 / room
- Privacy and security
  - No RF interception of the ultra-short range Communications.
  - Multi-Frequency, Multi-Mode dynamic Coding for wireless communications.
- Safety
  - Redundancy of the communications
  - Safe to hackers tentative.

Scope and ambition

The Connectivity roadmap will present the medium and long term applications and their impact for each communications sorted out category, and then will present the technology and design challenges to target these applications. At the end of the table the FOM formulae is given, and will be evaluated in the second part of the project.

Main Concepts

The next figure present the concept applied to the 5 years roadmap. At the centre of the figure the connectivity's families are sorted out taking into account the distance and the nature of the links. Two main natures are defined, either the link is guided, by extension we speak about Wireline, or the link is in the air, and then we speak about Wireless. 3 distance ranges separate the applications, if the distance is very short, and we speak about In Package and Device to Device communications; if the distance in in the centimetre metre to 100s metres range, we can put this category in the Indoor communications, afterward, from 100s metres to Kilometres we speak about Outdoor applications.

Sorting out the connectivity, we can define 6 different concepts, which will be presented on the next pages:

- The Outdoor Wireless Applications
- The Outdoor Wireline Applications
- The Indoor Wireless Applications
- The Indoor Wireline Applications
- The Device to Device Wireless Applications
- The In Package/Device Photonics Wireline Applications

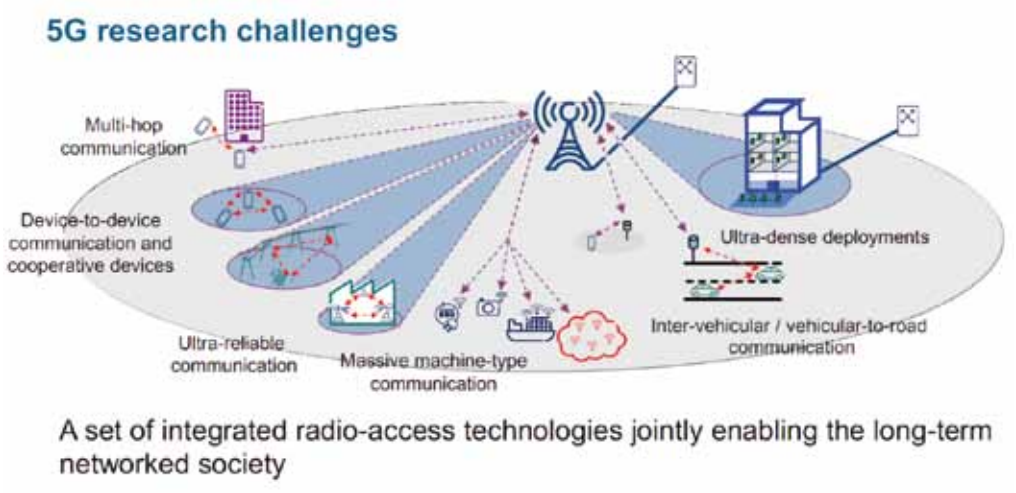


Fig. II.2.2: 5G and Beyond 5G Industrial vision (1)

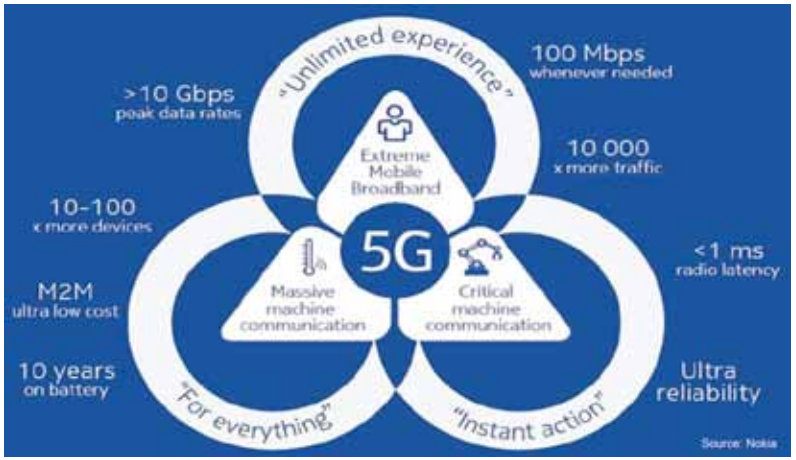


Fig. II.2.3: 5G and Beyond 5G Industrial vision (2)

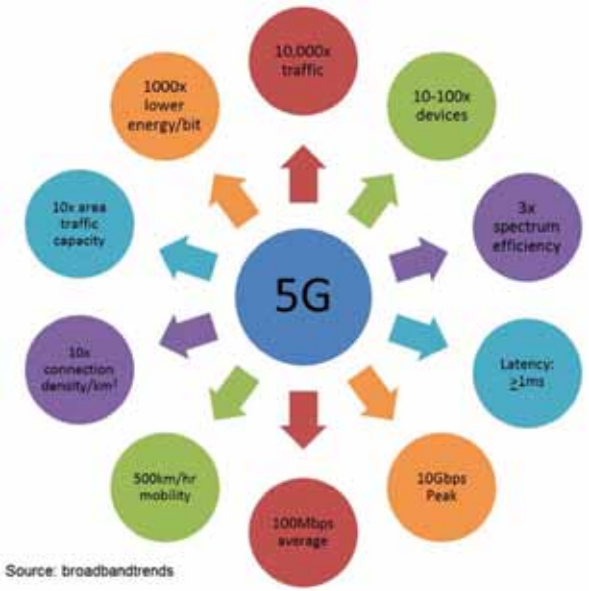


Fig. II.2.4: 5G and beyond 5G Specification

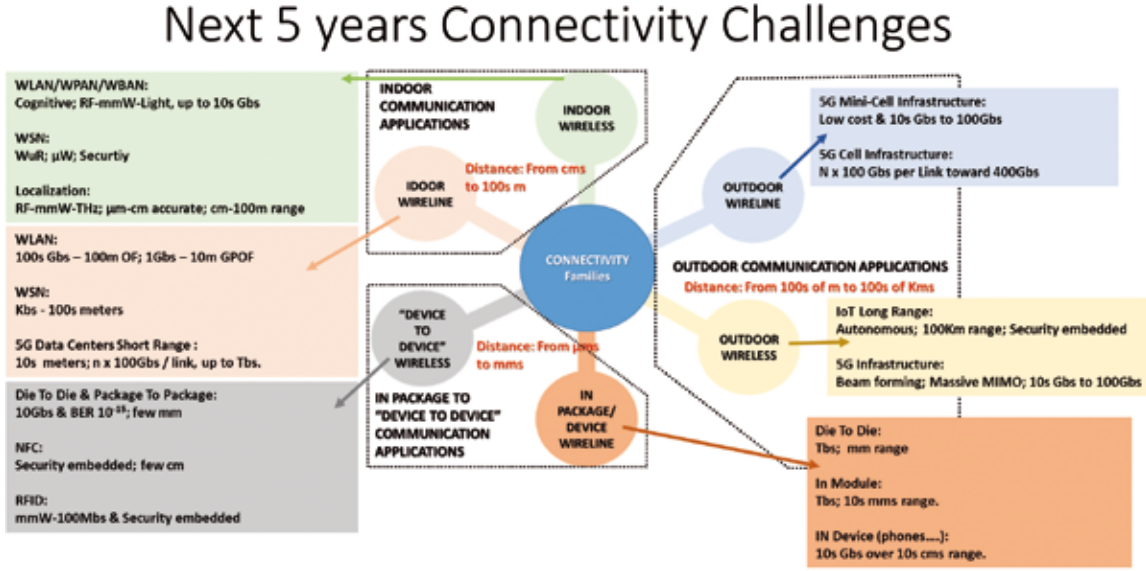


Fig. II.2.6: Connectivity families, and their main 5 years objectives.

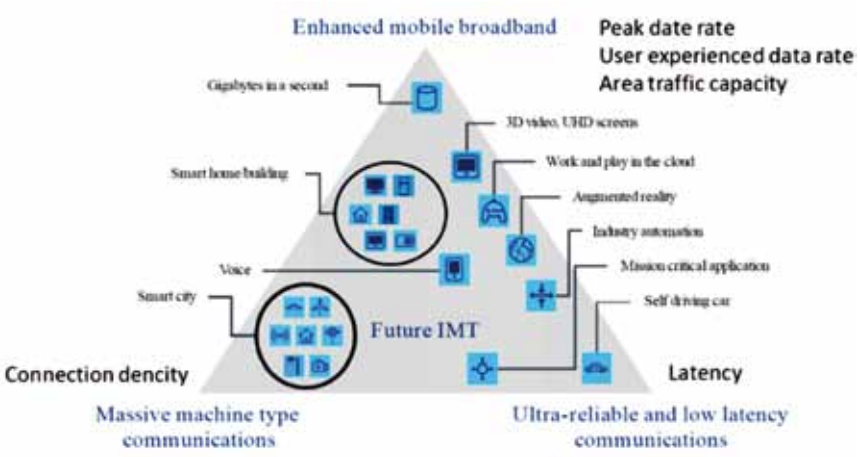


Fig. II.2.5: 5G and beyond 5G Specification

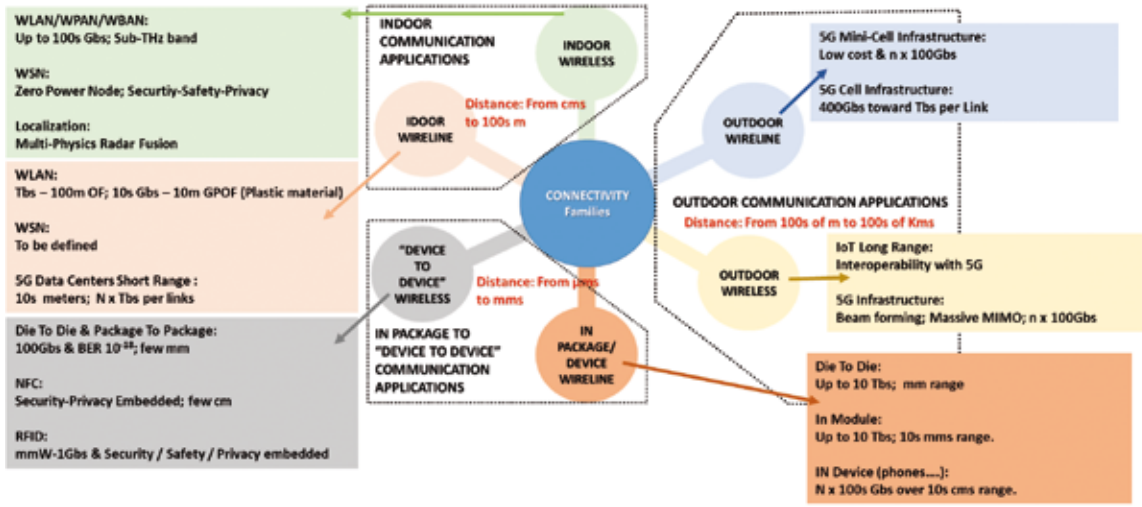


Fig. II.2.7: Connectivity families, and their main 10 years objectives.

Concept 1: OUTDOOR WIRELESS APPLICATIONS

Key research questions/issues

Technologies	Medium Term	Long Term
IoT Long Range	• Sub GHz (100 Km, Kbs & 15 km, Mbs) • Ultra low power (<mW)	• Sub GHz (100 Km, few Kbs & 15 km, few Mbs) Zero power (<100 µW) • Hardware security embedded.
Cellular Up & Down Links	• 0.7 to 100 GHz (10 Gbs) • With dynamic Beam Orientation	• Up to THz (10s of Gbs) • With Dynamic Beam Orientation
Fix Mini Cell to Mini Cell & Fix Mini Cell to Cell Backhauling	• mmW to THz bands (10s of Gbs) with Beam Focusing	• mmW to THz bands (100 Gbs) with Beam Forming

Application needs & Impact for Europe

Technologies	Medium Term	Long Term
5G+ Network	• Big Data, „Cloudification“: European solution for European Business and population.	• Full Distributed Cloud; Ad-hoc / opportunistic; local cloud (clustering); multi-cloud: European Independence.
Environmental survey	• Forests, water, snow …. Surveys: Better European Environment control.	• Global multi physics environment survey: Better disaster prevent.
Autonomous objects	• Driving aid, drones automation…: Lifes saved; injured number reduction; travel time reduction; CO_2 emission reduction.	• Dynamic automated data driven decision & vehicle action: Safe transport system. Sober transport system.

Technology and design challenges (1)

Power Amplifier Technology challenges	Medium Term	Long Term
F_{max}	More than 0.5 THz	More than 1 THz
Current density	More than 0.1A over wide gate area respecting F_{max}.	More than 0.1A over wide gate area respecting F_{max}.
Voltage breakdown	More than 5 V	More than 5 V
Linearity	High	Very High
Re-Configurability: Power Switch Transistors	Ron-Coff < 100 fs	Ron-Coff < 30 fs
Selectivity: Passives	High Q	Very High Q
Integration: Passives & Packages	Partially integrated in RDL	All integrated in the RDL level
Ultra-low capacitor ESD	Up to 30 GHz	Up to 100 GHz

Technology and design challenges (2)

Power Amplifier Design challenges	Medium Term	Long Term
Wide Band	Up to 5 GHz	Up to 10 GHz
PAE	Up to 40%	Up to 60%
mmW to THz	28 GHz to 86 GHz	Up to 180 GHz
Phase shifting	RF Step by step	RF continuously
Switch Band / Carrier frequency	Up to 5 GHz / up to 90 GHz	Up to 10 GHz / up to 180 GHz
RF and mmW ESD management	Up to 86 GHz	Up to 180 GHz
RF and mmW BIST	In the transceiver	At the Antenna Interface
RF and mmW Built In Self Control	In The Base Band	In the transceiver

Modulator – De-Modulator Technology challenges	Medium Term	Long Term
Re-Configurability: Multi-mode Multi frequencies transceivers:		
F_T	More than 0.5 THz	More than 1 THz
Variability	Allowing Design controlled	Allowing Design controlled
Components density	High (under 15 nm gate)	Very High (under 10 nm gate)
Switches Transistors	Ron-Coff < 50 fs	Ron-Coff < 10 fs
V_{dd}	Under 0.6 V	Under 0.4 V
I_{off}	Low.	Very Low.
Linearity	Very High	Extremely High
Selectivity: Passive	High Q	Very High Q
Capacitor density: Linear capacitor	High density per µm²	Very High density per µm²
ESD at high frequency and low voltage	Up to 86 GHz	Up to 180 GHz

Modulator – De-Modulator Design challenges	Medium Term	Long Term
Wide Band and High Dynamic ADCs at Low Power	Support MIMO 28 GHz/ 2Ghz BW	Support MIMO 180 GHz / 10 GHz BW
Design by Mathematics and Digital approach for Analog functions	Important	Mandatory
Reconfigurability to Cognitive Radio	Important	Mandatory
mmW power consumption reduction	10% versus present	50% versus present
Systematic BIST	Important	Mandatory
Built In Self Control	Nice to Have	Important

Concept 1: OUTDOOR WIRELESS APPLICATIONS

Technology and design challenges (3)

LNAs Technology Challenges	Medium Term	Long Term
NF_{min}	Less than 1 dB @ 100 GHz	Less than 1 dB @ 200 GHz
Linearity	High	Very High
Re-Configurability	Ron-Coff < 100 fs	Ron-Coff < 30 fs
Selectivity: Passives	High Q	Very High Q
Ultra-low Noise ESD	Up to 30 GHz	Up to 100GHz

LNAs Design Challenges	Medium Term	Long Term
Full Duplex Transceiver: TX isolation	More than 90 dB @ 6 GHz	More than 90 dB @ 100 GHz
Wide Band LNA	Up to 5 GHz	Up to 10 GHz
mmW to THz	28 GHz to 86 GHz	Up to 180 GHz
Frequency Tuning	10%	30%
Switch Band	4 Bands	10 Bands
Noise cancellation	Important	Mandatory
RF and mmW BIST	Important	Mandatory
RF and mmW Build In Self Control	Nice to Have	Important

Phase Frequency Generation Technology Challenges	Medium Term	Long Term
1/F noise: Cut Frequency	100s of Hz @ 6 GHz	100s of Hz @ 100 GHz
F_{max}	More than 0.5 THz	More Than 1 THz
Selectivity: Passives and resonators	High Q in GHz range	High Q in 10s of GHz range
Stability	Equivalent to Quartz but in GHz range	Equivalent to Quartz but in 10s of GHz range
Tuning range	15% Min	30% Min
Re-Configurability: Switch transistors	Ron-Coff < 50 fs	Ron-Coff < 10 fs
F_T	More than 0.5 THz	More Than 1 THz
Voltage breakdown	More than 2 V	More Than 2 V
Capacitor density: Linear Capacitor	High density per µm²	Very High density per µm²
Phase noise reduction	Important	Mandatory (by 6 to 9 dB)
White noise reduction	Important	Mandatory (by 30 to 36 dB)
VCO FOM	190 dBc/Hz/mW @ 6 GHz	195 dBc/Hz/mW @ 6 GHz

Phase Frequency Generation Design Challenges	Medium Term	Long Term
Frequency Agility	Nice to Have	Important
ADPLL	Important	Mandatory
Jitter noise reduction	Important	Mandatory
Reconfigurability	Nice to have	Important
Tunability	20%	40%

Technology and design challenges (4)

Antennas Technology Challenges:	Medium Term	Long Term
Dielectric Resonator Antennas	Low cost material @10 GHz	Low cost material @100 GHz
Lenses	Low cost mmW Lenses	Low cost sub-THz Lenses
Plastic antennas	Nice to have	Important
Polarization	Nice to Have	Important
Efficiency	High	Very High
Gain/ Antenna element	More than 0 dBi	More than 3 dBi

Antennas Design Challenges:	Medium Term	Long Term
Antennas Array	Mandatory	Mandatory
Mixed Array and Lenses	Important	Mandatory
Beam Forming: Dynamic orientation	Important	Mandatory
Tunability	20%	40%
Switched Bands	4	10

Other issues and challenges, interaction with other areas

- IoT Long Range: Standardization simplification (II.6); Life duration autonomy (II.3-5); Embedded security and artificial Intelligence (II.6); Integration (II.6); ultra-low cost (in cents range)
- Cellular Up & Dwn Links: Dynamic Beamforming (II.1; II.8); Privacy (II.6); Minimizing the Power consumption of the mobile (II.3-5), low cost in mobile (in $ range).
- Fix Backhauling: Up to 300 GHz spectrum (II.1; II.8); Wider Bands; Beamforming (II.6); Low cost solution (1/10 to 1/100 versus existing wireline solutions)

Definition of FoMs or planned evolution

FoM / Planned Evolution	2023	2026	2029	2033
IoT Long Range FOM: (15 km distance)	15 Gbs.m	30 Gbs.m	60 Gbs.m	120 Gbs.m
Cellular Up & Down Links FOM: (100 m distance)	50 Gbs.m	100 Gbs.m	800 Gbs.m	5000 Gbs.m
Fix Backhauling FOM: (150 m distance)	1500 Gbs.m	3750 Gbs.m	7500 Gbs.m	15000 Gbs.m

Concept 1: OUTDOOR WIRELESS APPLICATIONS

Competitive situation of concept 1

The Long Range IoT applications market is in high increase slope, and many standards are yet proposed in or outside of the 5GPPP association, we can site Sigfox, LoRa outside, LTE-M inside. Concerning the 5G wireless applications, the Cells to Cells communications are in competition with the wireline ones, there should be a balance between the wireless and the wireline market for these application, depending on the cell characteristics, small, and pico-cells base stations will use wireless, while big base station will continue to use wireline. The last 5G link between the mobile and the base market is in very high positive slope, as the number of users, and the bandwidth per user will increase and increase in the next years.

Recommendations for Concept 1

In this concept, we will have two different technology needs, the one for the IoT long range is oriented to the Ultra-Low power request, and the integration of all the functions in one node; the 5G wireless applications need high speed, high power, high bandwidth, and mmW, this means that technologies which will serve such applications are high end technologies.

Main challenges we will face to are the following:

- The Data conversion bottleneck: Tradeoff between the data volume to convert and the available power in a wearable device is not obvious to solve.
- The RF bandwidth and the mmW carrier frequencies requested by 5G and beyond 5G networks are not obvious to implement in low cost solutions based on Silicon materials.
- The Local Oscillator phase noise for Complex modulations requested by High data rate links in 5G and beyond 5G networks are very difficult to aim using low cost solutions based on Silicon materials.
- The SECURITY and the RELIABILITY are the main challenges targeting Vehicle Connectivity in the 5G and beyond 5G vision.

Technologies for Outdoor Wireless applications:

The present best technologies and devices are given in Fig. II.2.9, as we can read in this table, the low cost CMOS processes are absent of the best technical selection, even if, such technology is the lower costly one. If we analyze the trend, the CMOS processes can become the best choice for the IoT long Range Applications, but will be limited to the transceiver part of the other applications. The reduction of the cost of Radio interfaces (LNA, PA, Switches) and Local oscillators will come from the integration of III-V material on silicon substrate, (SOI) in the next 5 years, and in the integration of such III-V devices on CMOS over SOI substrate in the longer term. The mixt of exotic technologies and CMOS bring the breakthrough capacity of doing a local sense and control of the RF functions.

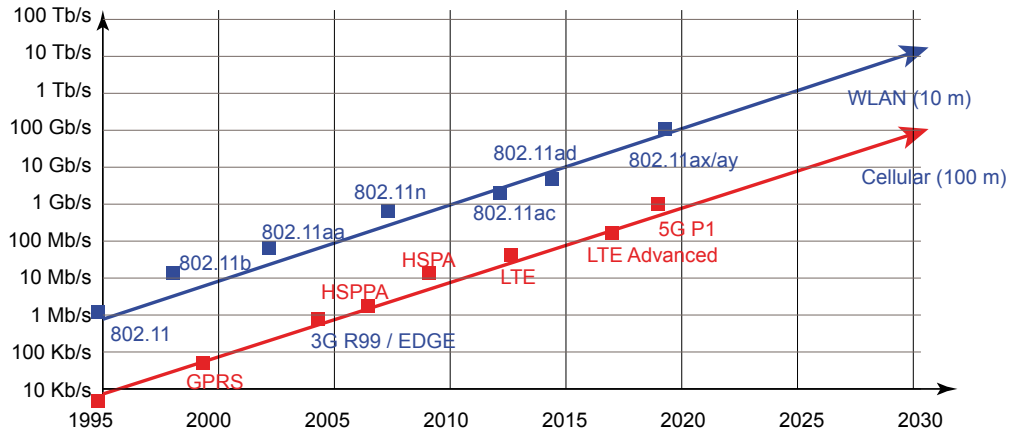


Fig. II.2.8: Outdoor Connectivity Roadmap.

	FOM		Key application	'Best' device
Speed	f_T	Cut-off of current gain	LNA	HEMT
	f_{max}	Cut-off of unilateral gain	VCO, PA,...	HEMT, HBT
	Ron * Coff	ON resistance * OFF capacitance	Switch	HEMT
Power	Pout	Output power	PA	GaN, HBT
	DE & PAE	Drain efficiency & power added efficiency	PA	
	BV	Breakdown voltage	PA	GaN, HBT, HEMT
	RF ruggedness	capability to withstand severe load mismatch conditions at high output-power levels	PA	HBT
Linearity	P1dB	1dB compression point	PA	HBT
	IIP3	3rd order intermodulation intercept point	LNA	
Noise	NFmin	Minimum noise figure	LNA	HBT, HEMT
	LF noise	Low frequency noise (1/f...)	VCO	HBT
Insertion loss		Passive components		III-V and SOI substrates

Fig. II.2.9: Outdoor Connectivity Roadmap.

Concept 2: OUTDOOR WIRELINE APPLICATIONS

Key research questions/issues

Technologies	Medium Term	Long Term
Cellular Base Station to Base Station	Optical fibers (100 Gbs/fiber)	Optic (200 Gbs/fiber)
Fix Mini Cell to Mini Cell, Fix Mini Cell to Cell Base Station	Low cost Optical Fibers (10s of Gbs) Through wall Plastic Waveguide (10 Gbs)	Low cost Optical Fibers (100 of Gbs) Through wall Plastic Waveguide (10s of Gbs)
Cell Base Station to Data Centers & Data Centers Long Range	Optical Fibers: 100 Gbs / fiber	Optical fibers: 200 Gbs / fiber
Long haul	Optical fibers: 40 Gbs / fiber	Optical Fibers: 100 Gbs / fiber

Application needs & Impact for Europe

Technologies	Medium Term	Long Term
5G+ Network & 5G+ Servers	Big Data, „Cloudification“: European solution for European Business and population	Full Distributed Cloud; Ad-hoc / opportunistic; local cloud (clustering); multi-cloud: European Independence
WWAN	Global Network: Web 3.0	Global Network: Web 4.0
F_{TTx}	Sub-Urban Network deployment: More Citizen will have RAN 2.0 access	Local Rural network deployment: Increasing the citizen number accessing to RAN 3.0.

Technology and design challenges

Optical Modulator or Laser Driver technology challenges	Medium Term	Long Term
F_T	More than 0.5 THz	More than 1 THz
Voltage breakdown	More than 2 V	More than 2 V
Linearity	High Voltage linearity	High voltage linearity
Re-Configurability	Ron-Coff < 100fs	Ron-Coff < 30fs

Optical Modulator Or Laser Driver Design challenges	Medium Term	Long Term
Multilevel Modulations	PAM4	PAM16 or better (PAM32 & XQAM)
Pre-emphasis capability	Important	Mandatory
Power consumed reduction	40% / bit	90% / bit

Modulations and Demodulation technology challenges	Medium Term	Long Term
Re-Configurability	Multimode	Multimode
F_T	More than 0.5 THz	More than 1 THz
Components density	High (under 15nm gate)	High (under 10nm gate)
Switch transistors	Ron-Coff < 50 fs	Ron-Coff < 10 fs
V_{dd}	Less than 0.6 V	Less than 0.4 V
I_{off}	Low	Very Low

Modulations and Demodulation Design challenges	Medium Term	Long Term
Multilevel Modulations	PAM4	PAM16 or better (PAM32 & XQAM)
Power consumed reduction	40% / bit	80% / bit
Equalization, Post emphasis	Important	Mandatory
CDR low power	Mandatory	Mandatory
Low jitter	BER 10-12	BER 10-15

Trans Impedance Amplifiers Technology challenges	Medium Term	Long Term
Current noise density	Low	Very Low
F_T	More than 0.5 THz	More than 1 THz
Re-Configurability	Ron-Coff < 50fs	Ron-Coff < 10fs
Linearity	High current linearity	Very high current linearity
Wide Band	Wide	Very Wide

Trans Impedance Amplifier Design Challenges	Medium Term	Long Term
TIA Sensitivity	-12 dBm	-15 dBm
High Dynamic range (Optical offset compensation)	Important	Mandatory

Frequency Generation And Clock Recovery Technology challenges	Medium Term	Long Term
F_{max}	More than 0.5 THz	More than 1 THz
Stability	High	Very High
Tuning range	30% Min	50% Min
Re-Configurability: Switch transistors	Ron-Coff < 50 fs	Ron-Coff < 10 fs
F_T	More than 0.5 THz	More than 1 THz
Voltage breakdown	More than 0.7 V	More than 0.5 V
Capacitor density: Linear Capacitor	High density per µm²	High density per µm²

Frequency Generation And Clock Recovery Design challenges	Medium Term	Long Term
Digital approach	Important	Mandatory
Ultra-Low Jitter	BER 10-12	BER 10-15
Stability	Quartz stability	Quartz to Optic resonator stability
Low Power High speed	1 decade improvement	2 decades improvement

Photodiode technology challenges	Medium Term	Long Term
Responsivity	0.85	0.95
Input capacitor	Few 10s fF	Few fF
Black current	Very low	Extremely Low
3D assembly	High efficiency	Very High efficiency

Concept 2: OUTDOOR WIRELINE APPLICATIONS

Laser Challenges	Medium Term	Long Term
Cost	Low (few $)	Very low (few 10s of cents)
Radiated Temperature	Low (less than 30 °C)	Very low (less than 10 °C)
Size	Small package	Very small (package)

Optical Modulators technology challenges	Medium Term	Long Term
Extinction ratio	6 dB	12 dB
Actuation	2V range actuation	1V range actuation.

Definition of FoMs or planned evolution

FoM / Planned Evolution	2023	2026	2029	2033
Cellular Base Station to Base Station FOM: 1 km distance	100 Gbs.Km	150 Gbs.km	200 Gbs.km	300 Gbs.km
Fix Mini Cell to Mini Cell, Fix Mini Cell to Cell Base Station FOM: 150 m distance	7500 Gbs.m	11000 Gbs.m	15000 Gbs.m	22000 Gbs.m
Cell Base Station to Data Centers & Data Centers Long Range FOM: 10 km distance	1000 Gbs.km	1500 Gbs.km	2000 Gbs.km	3000 Gbs.km
Long haul FOM: 100 km distance	4000 Gbs.km	7000 Gbs.km	10000 Gbs.km	14000 Gbs.km

Other issues and challenges, interaction with other areas

- Cellular Base Station to Base Station: Cost Reduction (II.6); Power consumption Reduction
- Fix Mini Cell to Mini Cell, Fix Mini Cell to Cell Base Station: Low cost solution (1/100 of present cell to cell; II.6); Low power solution (1/10 to 1/100 of present cell to cell)
- Cell Base Station to Data Centers & Data Centers Long Range: Data rate per Fiber (II.1; II.8); Complex modulations (II.6)
- Long haul: Data rate per Fiber (II.1; II.8); Complex modulations (II.6)

Competitive situation of Concept 2

The 5G wireline applications, from the Cells to Cells communications to long Haul communications are partially in competition with the wireless ones, for their "short range" part. In this range there should be a balance between the wireless and the wireline market for these application, depending on the cell characteristics, small, and pico-cells base stations will use wireless, while big base station will continue to use wireline. Concerning the other aspects, of wireline communications there is not any competitive solution nowadays.

Recommendations on Concept 2

The 5G wireline applications need high speed, high power, high bandwidth, and Photonics, this means that technologies which will serve such applications are high end technologies.

- TODAY: Cu vs Optics interconnection COST crossover point is at 10 Gbs and 1 m.
- TODAY, for DATA CENTERS, Active Optical Cables (AOCs) are used for anything longer than 3 m.
- TODAY, for HIGH PERFORMANCE COMPUTERS, photonic interconnections are used for anything longer than 0.05 m.

As data rates/channel exceed 100 Gbs, or where compelling advantages of photonics: lightweight, less power consumption, lower cost per bit, photonic interconnections will move inward the computer architecture.

Technologies for Outdoor Wireline applications

CMOS technology is the most used technology for the Transmitter, Receiver, and CDR building blocks and will benefit of the scaling in the next decade. The optic fibers will become the main wireline link components for high data rate communications. The optical/Electrical interfaces are using exotic technologies and will continue to use them, the silicon photonics will bring lower cost solutions in the next 5 – 10 years for the optical modulators, and optical resonators. The PIN diode and the Laser could benefit of these silicon optic technology innovative processes. One of the main challenge in silicon photonics is the integration, and the packaging.

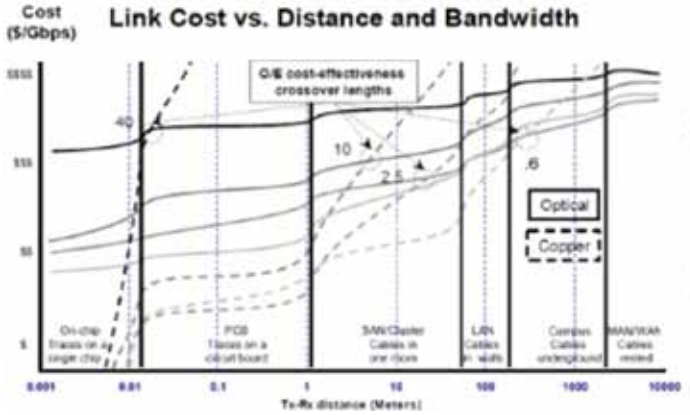


Fig. II.2.10: Optic Fibre / Copper economic trade off

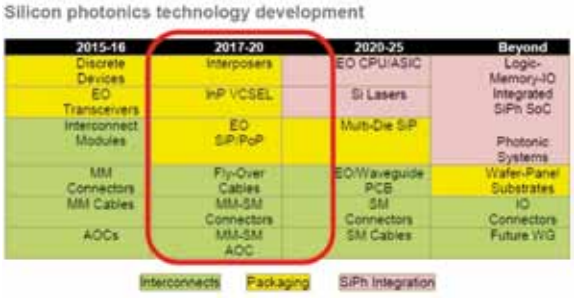


Fig. II.2.11: Silicon Photonic Technology Roadmap

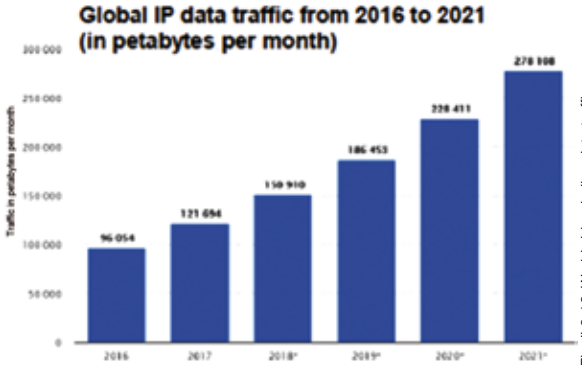


Fig. II.2.12: Worldwide wireline data traffic

Concept 3: INDOOR WIRELESS APPLICATIONS

Key research questions/issues

Technologies	Medium Term	Long Term
WLAN/ WPAN/ WBAN	Cognitive Multi Mode Radio 0-6 GHz and 60 GHz band LiFi (10s Gbs) P2P over 100 GHz bands New sub-THz band	Cognitive Multi Mode WLAN over 100 GHz LiFi (100s Gbs) P2P in sub-THz band
WSN	Cooperative sensing, cooperative radio Toward „Zero Power“ Hardware Securtiy embedded.	„Recycling material“ for radio „Zero power node“ Security / Safety / Privacy Embedded.
Localization	Radar (RF to THz) UWB Ultrasound Impulse light	Multi physics fusion

Application needs & Impact for Europe

Technologies	Medium Term	Long Term
Fitness	Performance sensing & benchmarks: Consumer Market	Enhanced human performances: Consumer Market
Healthcare	E-Monitoring: Aging people maintained at home.	E-Hospital: Specialist intervention through the Net. Data Analysis and decision making.
Home safety & security	E-Survey: Domestic accidents and burglaries prevention	Autonomous Home protection: Data Analysis and decision making
Public space safety & security	E-Survey: aggressions, theft, terrorist actions preventing.	Autonomous Public Protection: Multi source data analysis and decision making.
Factory 4.0	Machine automation: reduction of human intervention in production process.	Factory 4.0: No Human intervention.
Autonomous objects	Mono-function autonomous machine: Reducing borrow tasks at home.	CPS: First generation of multi functions robots.

Technology and design challenges

Power Amplifier Technology challenges	Medium Term	Long Term
Fmax	More than 0.5 THz	More than 1 THz
Voltage breakdown	More than 2 V	More than 2 V
Linearity	High	Very High
Re-Configurability: Power Switch Transistors	Ron-Coff < 100 fs	Ron-Coff < 30 fs
Selectivity: Passives	High Q	Very High Q

Power Amplifier Design challenges	Medium Term	Long Term
Wide Band	Up to 10 GHz	Up to 20 GHz
PAE	Up to 50%	Up to 60%
mmW to THz	Up to 100 GHz	Up to 300 GHz
Phase shifting	Nice to have	Important
Switch Band	Important	Mandatory

Modulator – De-Modulator Technology challenges	Medium Term	Long Term
Time and Frequency domain Approach		
F_T	More than 0.5THz	More than 1 THz
Variability	Allowing Design controlled	Allowing Design controlled
Components density	High (under 15 nm gate)	Very High (under 10 nm gate)
Switches Transistors	Ron-Coff < 50 fs	Ron-Coff < 10 fs
V_{dd}	Under 0.6 V	Under 0.4 V
I_{off}	Low	Very Low
Current Inversion Analog Approach		
F_T	More than 0.5 THz	More than 1 THz
Variability	Very low in weak inversion	Very low in weak inversion
Linearity	High	High
Selectivity: Passive	High Q	Very High Q
Capacitor density: Linear capacitor	High density per µm²	Very High density per µm²

Modulator – De-Modulator Design challenges	Medium Term	Long Term
Design by Mathematics and Digital approach for Analog functions	Nice to have	Important
Reconfigurability to Cognitive Radio	Nice to have	Important
Weak inversion design	Important	Mandatory
RF & mmW in die	Important	Mandatory

LNAs Technology Challenges	Medium Term	Long Term
NF_{min}	Less than 1 dB @ 100 GHz	Less than 1 dB @ 200 GHz
Linearity	High	Very High
Re-Configurability	Ron-Coff < 100 fs	Ron-Coff < 30 fs
Selectivity: Passives	High Q	Very High Q

LNAs Design Challenges:	Medium Term	Long Term
Full Duplex Transceiver: TX isolation	More than 90 dB @ 6 GHz	More than 90 dB @ 100 GHz
Wide Band LNA	Up to 10 GHz	Up to 20 Ghz
mmW to THz	Up to 100 GHz	Up to 300 GHz
Frequency Tuning	15%	30%
Switch Band	Important	Mandatory
Noise cancellation	Nice to have	Important

Concept 3: INDOOR WIRELESS APPLICATIONS

Phase Frequency Generation Technology Challenges	Medium Term	Long Term
1/F noise: Cut Frequency	100s of Hz	10s of Hz
F_{max}	More than 0.5 THz	More Than 1 THz
Selectivity: Passives and resonators	High Q in GHz range	High Q in 10s of GHz range
Stability	Equivalent to Quartz but in GHz range	Equivalent to Quartz but in 10s of GHz range
Tuning range	15% Min	30% Min
Re-Configurability: Switch transistors	Ron-Coff < 50 fs	Ron-Coff < 10 fs
F_T	More than 0.5 THz	More Than 1 THz
Voltage breakdown	More than 2 V	More Than 2 V
Capacitor density: Linear Capacitor	High density per µm²	Very High density per µm²

Phase Frequency Generation Design Challenges	Medium Term	Long Term
Frequency Agility	Nice to have	Important
ADPLL	Important	Mandatory
Phase noise reduction	Nice to have	Important
White noise reduction	Nice to have	Important
Reconfigurability	Nice to have	Important
Tunability	15%	30%

Antennas Technology Challenges	Medium Term	Long Term
Antenna on die with Semi-conductor substrate	0 dBi gain and λ/n design approach	0 dBi gain and λ/2n design approach
Antenna in Package on Organic substrate	Low cost mmW	Low cost sub-THz
Antenna in a Module on ceramic substrate	Low cost mmW	Low cost sub-THz
Antenna on Other Metamaterial	Low cost mmW	Low cost sub-THz

Antennas Design Challenges	Medium Term	Long Term
Antennas Array	Important	Mandatory
Antenna with reflectors	Nice to have	Important
Beam Forming: Dynamic orientation	Important	Mandatory
Tunability	15%	30%
Switched Bands	Important	Mandatory

Definition of FoMs or planned evolution

FoM / Planned Evolution	2023	2026	2029	2033
WLAN FOM: (10 m)	250 Gbs.m	500 Gbs.m	1000 Gbs.m	2000 Gbs.m
WPAN FOM: (10 m)	50 Mbs.m	100 Mbs.m	150 Mbs.m	200 Mbs.m
WBAN FOM: (1 m)	1 Kbs.m	10 Kbs.m	100 Kbs.m	1000 Kbs.m
WSN FOM: (10 m)	10 Kbs.m	100 Kbs.m	1000 Kbs.m	10000 Kbs.m
Localization FOM: (10 m) FOM is relative accuracy	1%	0.3%	0.05%	0.01%

Other issues and challenges, interaction with other areas

- WLAN: mmW to THz spectrum use (II.1; II.8); Beam forming (II.6); Privacy (II.6); Wide band; Low cost (in $ range); Integration (II.6)
- WPAN: Embedded Security (II.6); Low Power (mW range); Integration (II.6); Low cost (in 10s of cents range)
- WBAN: Embedded security(II.6); Privacy (II.6); Ultra low power (100 µW range); Bio-compatible Integration (II.6)
- WSN: Embedded security (II.6); Ultra low power (Life duration Autonomy; WP4); Integration (II.6); Ultra low cost (in cents range)
- Localization : Spectrum compatibility (II.6); data fusion (II.6); Integration (II.6)

Competitive situation of Concept 3

The Indoor wireless applications, from WBAN to WLAN through WSN are very open, a huge standard competition is ongoing, and the win standards are not yet known. Whatever, all of these applications need the same technology offer.

Recommendations for Concept 3

From the in the WSN to the WLAN all these applications request Energy efficiency and are oriented to the Low power to Ultra-Low power request, finally, they will integrate all the functions in a SOC approach.

Challenges

- Smart wearables devices
  will aim Ultra-light, low power, waterproof sensors integrated in people's clothing or patches : low power and robust sensors, overall management.
- Sensors networks for Smart cities, building
  … will aim Low power networks, energy efficiency
- Mobile Video Surveillance
  On aircrafts, drones, cars, railways … will need highly reliable and secure networks.
- The Life duration Autonomous sensor
  … is the next big challenge for wireless sensor networks.
- The power efficiency, data throughput and range reconfigurability, and security privacy
  … are the main challenges for WLAN networks in SOC approaches.

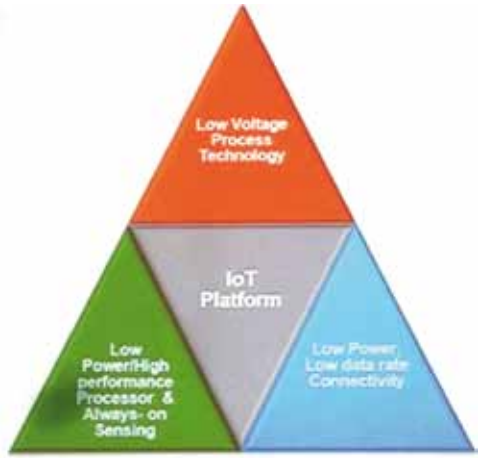


Fig. II.2.13: IoT Technology challenges

Concept 3: INDOOR WIRELESS APPLICATIONS

Technologies for Indoor Wireless applications

CMOS technology processes are the main circuit integration technology used and will continue to be the most used for all the components of the Indoor Wireless applications, circuits will benefit from the scaling to improve their operating frequency. The necessities will be supplied by SOI technologies allowing medium power output with FET stacking architectures. Challenge in this field will be the 3D integration from the digital Medium Access communication processing to the Electromagnetic radiation (antennas) in one low cost package. Organic materials are the best candidate from the economic point of view, if they can demonstrate their technical capability to answer to the stringent specifications of such applications.

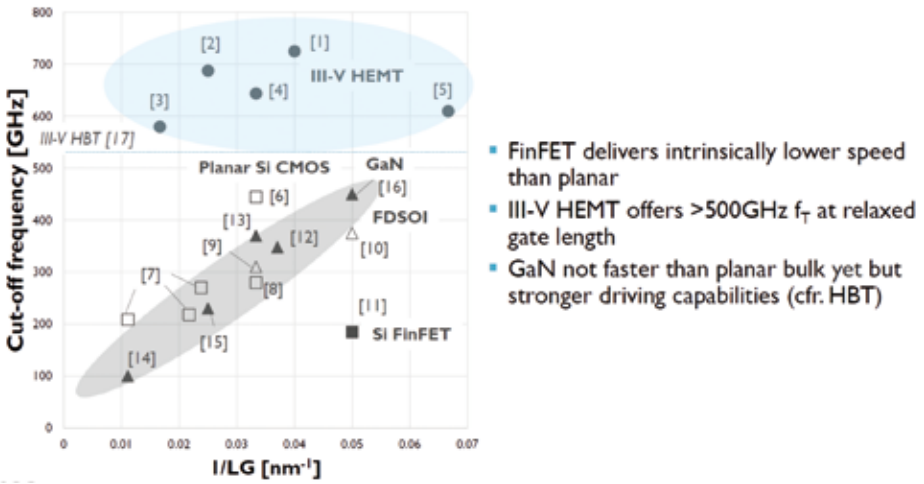


Fig. II.2.14: Silicon and III-V technologies for Wireless

Concept 4: INDOOR WIRELINE APPLICATIONS

Key research questions/issues

Technologies	Medium Term	Long Term
WLAN	• Copper (Low power HDR); PLC (100 Mbs; 20 m); Optical Fiber (100 Gbs; 100 m); GI-POF (1 Gbs; 10m); mmW Plastic Wave Guide (few Gbs; <20 m) • Copper (1 m; 10 s of Gbs); Optical Fiber (10 m; 400 Gbs/fiber); GI-POF (1 m; 1 Gbs)	• Copper (ULP HDR); PLC (n x 100 Mbs; 20 m); Optical Fiber (100 s of Gbs; 100 m); GI-POF (10 Gbs; 10 m); mmW PWG (n x 10 Gbs; <20 m) • Copper (1 m; 100 Gbs) ; Optical Fiber (10 m; 1 Tbs/fiber); GI-POF (1 m; 10 Gbs)
Data Centers Short Range	mmW PWG(1 m; 10 Gbs)	THz PWG (1 m; 10 s of Gbs)

Application needs & Impact for Europe

Technologies	Medium Term	Long Term
Home Automation	Multi physics Network: Reducing time transfer for data at home.	Multi physics Network: Reducing decision making at home.
Factory Automation	Multi physics Network: Reducing time transfer for data in Factory	Multi physics Network: for Factory 4.0
5G+ Data Center	Very high speed Network: for short range transfer.	Very high speed Network: for RAN 3.0

Technology and design challenges

Optical Modulator Or Coper line Driver technology challenges	Medium Term	Long Term
F_T	More than 0.5 THz	More than 1 THz
Voltage breakdown	More than 2 V	More than 2 V
Linearity	High Voltage linearity	High voltage linearity
Re-Configurability	Ron-Coff < 100 fs	Ron-Coff < 30 fs

Optical Modulator Or Coper line Driver Design challenges	Medium Term	Long Term
Multilevel Modulations	DP-16QAM	DP-64QAM
Pre-emphasis capability	Important	Mandatory
Power consumed reduction	20%	40%

Modulations and Demodulation technology challenges	Medium Term	Long Term
Re-Configurability	Multimode	Multimode
F_T	More than 0.5 THz	More than 1 THz
Components density	High (under 15 nm gate)	High (under 10 nm gate)
Switch transistors	Ron-Coff < 50 fs	Ron-Coff < 10 fs
V_{dd}	Less than 0.6 V	Less than 0.4 V
I_{off}	Low	Very Low

Concept 4: INDOOR WIRELINE APPLICATIONS

Modulations and Demodulation Design challenges	Medium Term	Long Term
Multilevel Modulations.	DP-16QAM	DP-64QAM
Power consumed reduction	20%	40%
Equalization, Post emphasis	Important	Mandatory
CDR low power	Digital + LC resonator	Digital + Optical resonator
Low jitter	BER 10-12	BER 10-15

Trans Impedance Amplifiers Technology challenges	Medium Term	Long Term
Current noise density	Low	Very Low
F_T	More than 0.5 THz	More than 1 THz
Re-Configurability	Ron-Coff < 50 fs	Ron-Coff < 10 fs
Linearity	High current linearity	Very high current linearity
Wide Band	Wide	Very Wide

Trans Impedance Amplifier Design Challenges	Medium Term	Long Term
TIA sensitivity	-12 dBm	-15 dBm
High Dynamic range (Optical offset compensation)	Important	Mandatory

Frequency Generation And Clock Recovery Technology challenges	Medium Term	Long Term
F_{max}	More than 0.5 THz	More than 1 THz
Stability	High	Very High
Tuning range	30% Min	50% Min
Re-Configurability: Switch transistors	Ron-Coff < 50 fs	Ron-Coff < 10 fs
F_T	More than 0.5 THz	More than 1 THz
Voltage breakdown	More than 0.7 V	More than 0.5 V
Capacitor density: Linear Capacitor	High density per µm²	High density per µm²

Frequency Generation And Clock Recovery Design challenges	Medium Term	Long Term
Digital approach	Important	Mandatory
Ultra-Low Jitter	BER 10-12	BER 10-15
Stability	Quartz	Quartz or Optical resonator
Low Power High speed	1 decade	2 decade

Photodiode technology challenges:	Medium Term	Long Term
Responsivity	0.85	0.95
Input capacitor	Few 10s fF	Few fF
Black current	Very low	Extremely Low
3D assembly	High efficiency	Very High efficiency

Laser Challenges:	Medium Term	Long Term
Cost	Low (few 10s of cents)	Very low (few cents range)
Radiated Temperature	Low (less than 10 °C)	Very low (less than 5 °C)
Size	Small (Over die integration)	Very small (over die integration)

Optical Modulators technology challenges:	Medium Term	Long Term
Extinction ratio	6 dB	12 dB
Actuation	2 V range actuation	1 V range actuation.

Definition of FoMs or planned evolution

FoM / Planned Evolution	2023	2026	2029	2033
WLAN FOM: (10 m)	1000 Gbs.m	1500 Gbs.m	2000 Gbs.m	3000 Gbs.m
WSN FOM: (10 m)	500 Mbs.m	1000 Mbs.m	1500 Mbs.m	2000 Mbs.m
Data Centers Short Range FOM: (10 m)	4000 Gbs.m	7000 Gbs.m	10000 Gbs.m	15000 Gbs.m

Other issues and challenges, interaction with other areas

- WLAN: Integration (II.6); low cost (in the wireless solutions range: $)
- WSN: Low cost (in the wireless solutions range: cents); Integration (II.6)
- Data Centers Short Range: Data Rate per fiber (II.1 II.8); Integration (II.6); Reliability (II.6)

Competitive situation of Concept 4

Indoor wireline Market is driven by the Data centre (in orange in the graph below), and next decade data traffic increase concentrate the internal data centre links to optical fibres technologies, actually, Silicon photonics processes will be the main winners in market share, if they can answer to the specifications challenges (See Fig. II.2.15, next page).

Recommendations for Concept 4

As the data rate will dramatically increase, cost and power per bit will be the main market challenges, a first estimation given in the following table shows that we would expect less than 10 cents per Gbs with a total of 12 pJ/b per link to satisfy Exascale data rate, where the present performances are between 1 and 3 $ per Gbs with 30 to 40 pJ/b per link (See Fig. II.2.16).

Concept 4: INDOOR WIRELINE APPLICATIONS

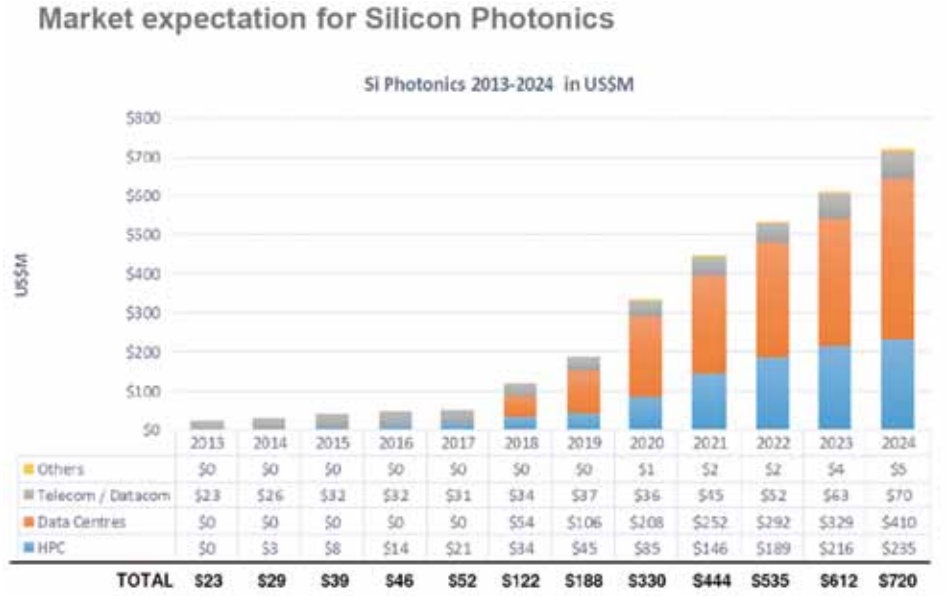


Fig. II.2.15: Indoor Data Com specifications and Market

Technologies for Indoor Wireline applications

CMOS technology is the most used technology for the Transmitter, Receiver, and CDR building blocks and will benefit of the scaling in the next decade. The optic fibers will become the main wireline link components for such very high data rate communications. The optical/ Electrical interfaces are using exotic technologies and will continue to use them, the silicon photonics will bring lower cost solutions in the next 5 – 10 years for the optical modulators, and optical resonators.
One of the main challenge in silicon photonics is the integration, and the packaging.

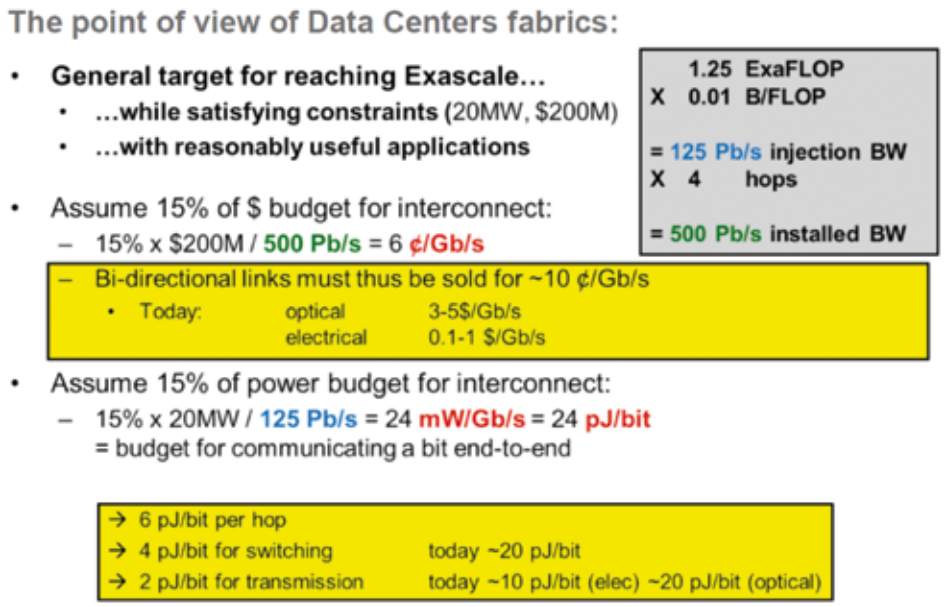


Fig. II.2.16: Economic challenges for Indoor Wireline

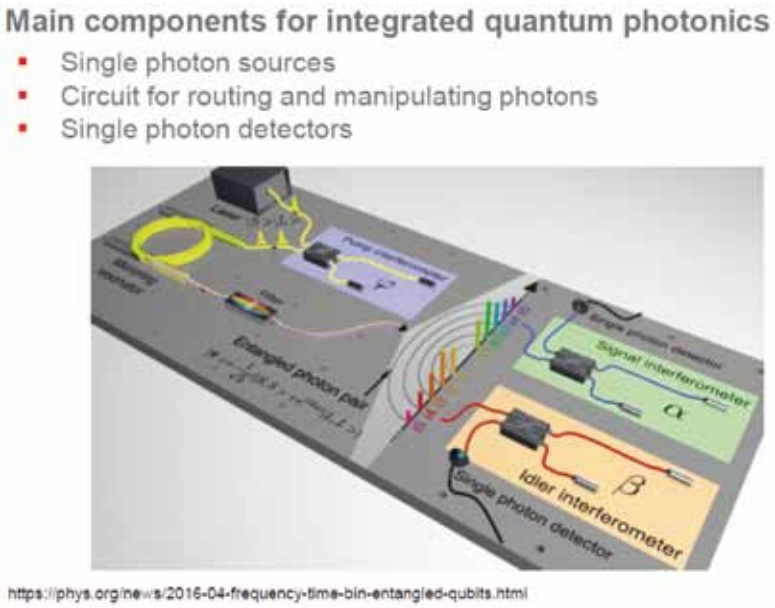


Fig. II.2.17: Technology challenge for Indoor Wireline

Concept 5: DEVICE TO DEVICE WIRELESS APPLICATIONS

Key research questions/issues

Technologies	Medium Term	Long Term
Die To Die & Package To Package	• Data Rate > 10 Gbs; BER 10-15	Data Rate > 100 Gbs; BER 10-18
NFC	• RF (13 MHz; 1 Mbs); Hardware Security Embedded • RF (13 MHz; 100 Kbs); RF (2.4 GHz; 10 Mbs); mmW (60 GHz; 100 Mbs)	Security / Privacy Embedded
RFID	• Hardware Security Embedded	Security / Safety / Privacy Embedded

Application needs & Impact for Europe

Technologies	Medium Term	Long Term
High data rate without contact transfer	Multi-media transfer: Consumer market.	Data-Base transfer: Consumer market.
Uncontacted Safe Data transfer	Money transfer: Security of the operation.	Personal and confidential data transfer: Safe and secure.
Traceability and identification	Goods and animals: safe and secure	People: Privacy.

Technology and design challenges

Power Amplifier Technology challenges	Medium Term	Long Term
F_{max}	More than 0.5 THz	More than 1THz
Voltage breakdown	More than 2 V	More than 2 V
Re-Configurability: Power Switch Transistors	Ron-Coff < 100 fs	Ron-Coff < 30 fs

Power Amplifier Design challenges	Medium Term	Long Term
mmW to THz	Up to 50 GHz	Up to 100 GHz
Switch Band	Important	Mandatory

Modulator – De-Modulator Technology challenges	Medium Term	Long Term
Digital Approach		
F_T	More than 0.5 THz	More than 1 THz
Variability	Allowing Design controlled	Allowing Design controlled
Components density	High (under 15 nm gate)	Very High (under 10 nm gate)
Switches Transistors	Ron-Coff < 50 fs	Ron-Coff < 10 fs
V_{dd}	Under 0.6 V	Under 0.4 V
I_{off}	Low	Very Low

Modulator – De-Modulator Design challenges	Medium Term	Long Term
Design by Mathematics and Digital approach for Analog functions	Mandatory	Mandatory
Reconfigurability	Mandatory	Mandatory

LNAs Technology Challenges	Medium Term	Long Term
NF_{min}	Less than 2 dB @ 50 GHz	Less than 2 dB @ 100 GHz
Re-Configurability	Ron-Coff < 100 fs	Ron-Coff < 30 fs

LNAs Design Challenges	Medium Term	Long Term
mmW to THz	Up to 50 GHz	Up to 300 GHz
Switch Band	Important	Mandatory

Phase Frequency Generation Technology Challenges	Medium Term	Long Term
1/F noise: Cut Frequency	100s of Hz	10s of Hz
F_{max}	More than 0.5 THz	More Than 1THz
Tuning range	15% Min	30% Min
Re-Configurability: Switch transistors	Ron-Coff < 50 fs	Ron-Coff < 10 fs
F_T	More than 0.5 THz	More Than 1THz
Capacitor density: Linear Capacitor	High density per µm²	Very High density per µm²

Phase Frequency Generation Design Challenges	Medium Term	Long Term
ADPLL	Mandatory	Mandatory
Reconfigurability	Mandatory	Mandatory

Antennas Technology Challenges	Medium Term	Long Term
Antenna on die with Semi-conductor substrate	-3 dBi, up to 50 GHz	-3 dBi, up to 100 GHz
Antenna in Package on Organic substrate	6 dBi, up to 50 GHz	6 dBi, up to 100 GHz

Antennas Design Challenges	Medium Term	Long Term
Antenna with reflectors	18 dBi, up to 50 GHz	18 dBi, up to 100 GHz
Switched Bands	Important	Mandatory

Definition of FoMs or planned evolution

FoM / Planned Evolution	2023	2026	2029	2033
Die To Die & Package To Package FOM: (10 cm)	1 Gbs.m	5 Gbs.m	10 Gbs.m	50 Gbs.m
NFC FOM: (10 cm)	0.1 Mbs.m	0.5 Mbs.m	1 Mbs.m	5 Mbs.m
RFID FOM: (1 m)	100 Mbs.m	500 Mbs.m	1000 Mbs.m	1500 Mbs.m

FOM = Data_rate(Gbs, or Mbs)×D(m)

Concept 5: DEVICE TO DEVICE WIRELESS APPLICATIONS

Other issues and challenges, interaction with

- Die To Die & Package To Package : In the wireline quality: 10E-18 BER; Integration density (II.8); Ultra-low power (II.3-5) (<mW/link)
- NFC: Privacy (II.6); Embedded security (II.6); power consumption (II.3-5)
- RFID: mmW spectrum use (II.1); Embedded security (II.6); Ultra-low power (II.3-5) (<mW); Integration (II.6)

Competitive situation of Concept 5

RFID and NFC are the main drivers of such markets, the positive slope will continue and will be reinforced, with the request of identifications, the request of food security, the request of safe and secured bank data transfers, and so on, mmW is a new market expansion possibility. The die to die market, is a wireless niche market, the stringent BER requested being not in line with the present wireless performances.

Recommendations for Concept 5

RFID and NFC applications request Energy efficiency and are oriented to Ultra-Low power request, they will integrate all the functions including security stuff in a SOC approach. The last die to die and in package applications request in addition high bandwidth, and high frequency to mmW capabilities.

Technologies for the in package wireless applications

CMOS processes are the main used technology for such applications and will be the main ones in the future. The innovative field is mainly in the antenna requests and their implementation.

Concept 6: IN PACKAGE/DEVICE PHOTONICS WIRELINE APPLICATIONS

Key research questions/issues

Technologies	Medium Term	Long Term
Die 2 Die	• Copper links (100 Gbs, 100s um) • Photonics Silicon Interposer (1 Tbs, 10s mms) • Active Interposers (100 Gbs, mm) Flip chipped + Copper (100 Gbs , mm)	• Photonic Silicon Interposer more than 2 Tbs over 10s mm • Active Interposers (1 Tbs, mm)
Module 2 Module	• Optical Waveguide (Tbs, 10 cm) • Multifiber connectors, passive alignment	Toward 10 Tbs over 10 cm
Active cable	• Optical guide/Fiber (toward 2Tbs, 10s cm) • GI-POF (10Gbs, 10s cms) • mmW Plastic Wave Guide (10s Gbs, 10s cm)	Toward 10 Tbs over 10s cms

Application needs & Impact for Europe

Technologies	Medium Term	Long Term
HPC:	Multicore Processor: European Independence.	Cognitive computing: European Independence.
5G+ Data-center	Big data	Big Data
Intelligent transport; Entertainment; Factory 4.0…	Data transfer	Data transfer

Technology and design challenges

Optical Modulator or laser driver technology challenges	Medium Term	Long Term
F_T	More than 0.5 THz	More than 1 THz
Voltage breakdown	More than 2 V	More than 2 V
Linearity	High Voltage linearity	High voltage linearity
Re-Configurability	Ron-Coff < 100 fs	Ron-Coff < 30 fs

Optical Modulator or laser Design challenges	Medium Term	Long Term
Multilevel Modulations	64 QAM	256 QAM and more
Pre-emphasis capability	Mandatory	Mandatory
Power consumed reduction	20%	40%

Modulations and Demodulation technology challenges	Medium Term	Long Term
F_T	More than 0.5 THz	More than 1 THz
Components density	High (under 15 nm gate)	High (under 10 nm gate)
Switch transistors	Ron-Coff < 50 fs	Ron-Coff < 10 fs
V_{dd}	Less than 0.6 V	Less than 0.4 V
I_{off}	Low	Very Low

Concept 6: IN PACKAGE/DEVICE PHOTONICS WIRELINE APPLICATIONS

Modulations and Demodulation Design challenges	Medium Term	Long Term
Multilevel Modulations.	64 QAM	256 QAM and more
Power consumed reduction	20%	40%
Equalization, Post emphasis	Mandatory	Mandatory
CDR low power	Digital + Optic resonator	Digital + Optic resonator
Low jitter	BER 10-15	BER 10-18

Trans Impedance Amplifiers Technology challenges	Medium Term	Long Term
Current noise density	Low	Very Low
F_T	More than 0.5 THz	More than 1 THz
Re-Configurability	Ron-Coff < 50 fs	Ron-Coff < 10 fs
Linearity	High current linearity	Very high current linearity
Wide band	Wide	Very Wide

Trans Impedance Amplifier Design Challenges	Medium Term	Long Term
TIA sensitivity	-15 dBm	-18 dBm
High Dynamic range (Optical offset compensation)	Mandatory	Mandatory

Frequency Generation And Clock Recovery Technology challenges	Medium Term	Long Term
F_{max}	More than 0.5 THz	More than 1 THz
Stability	High	Very High
Tuning range	30% Min	50% Min
Re-Configurability: Switch transistors	Ron-Coff < 50 fs	Ron-Coff < 10 fs
F_T	More than 0.5 THz	More than 1 THz
Voltage breakdown	More than 0.7 V	More than 0.5 V
Capacitor density: Linear Capacitor	High density per µm²	High density per µm²

Frequency Generation And Clock Recovery Design challenges	Medium Term	Long Term
Digital approach	Mandatory	Mandatory
Ultra-Low Jitter	BER 10-15	BER 10-18
Stability	Optic Resonator	Optic Resonator or better
Low Power High speed	1 decade	2 decade

Photodiode technology challenges	Medium Term	Long Term
Responsivity	0.85	0.95
Input capacitor	Few 10s fF	Few fF
Black current	Very low	Extremely Low
3D assembly	High efficiency	Very High efficiency

Laser Challenges	Medium Term	Long Term
Integration in Photonic Silicon	III-V/Si	Ge Laser and other Si compatible

Optical Modulators technology challenges	Medium Term	Long Term
Extinction ratio	6 dB	12 dB
Actuation	Less than 2 V range actuation	In 1V range actuation

Optical Switches Challenge	Medium Term	Long Term
	Research	Development

Definition of FoMs or planned evolution

FoM / Planned Evolution	2023	2026	2029	2033
Die 2 Die FOM: (1 cm distance)	10 Gbs.m	15 Gbs.m	20 Gbs.m	30 Gbs.m
Module 2 Module FOM: (10 cm distance)	100 Gbs.m	500 Gbs.m	1000 Gbs.m	5000 Gbs.m
Device 2 Device FOM: (1 m distance)	1000 Gbs.m	5000 Gbs.m	10000 Gbs.m	50000 Gbs.m

Other issues and challenges, interaction with other areas

- Die 2 Die : Photonic integration (II.1, II.2, II.6, II.8); Power consumption (<mW / link) (II.3-5); Heat management (II.6)
- Module 2 Module : Photonic integration (II.1, II.2, II.6, II.8) ; Power consumption (in the mW range) (II.3-5)
- Device 2 Device : Photonic integration (II.1, II.2, II.6, II.8); Power consumption (in the 10s of mW range) (II.3-5)

Competitive situation of Concept 6

This photonics communications are the main promising techniques to implement in a package high speed network. The roadmap is clear and defined. We can't speak about High Performance Computing without such connectivity. In the following graph, the blue part of the market is dedicated to such technology if it meets the technical challenges (See Fig. II.2.18).

Recommendations for Concept 6

The photonics communications need high speed, medium power, high bandwidth, and Photonics components, this means that technologies which will serve such applications are high end technologies.

Technologies for In package, on board optic wireline

Circuit will definitively be done with CMOS technologies, where the scaling will bring speed and frequencies to the functions, I/O interfaces and Local oscillators will benefit from the silicon photonics development, and one of the main challenges is in the packaging solutions of such applications.

Concept 6: IN PACKAGE/DEVICE PHOTONICS WIRELINE APPLICATIONS

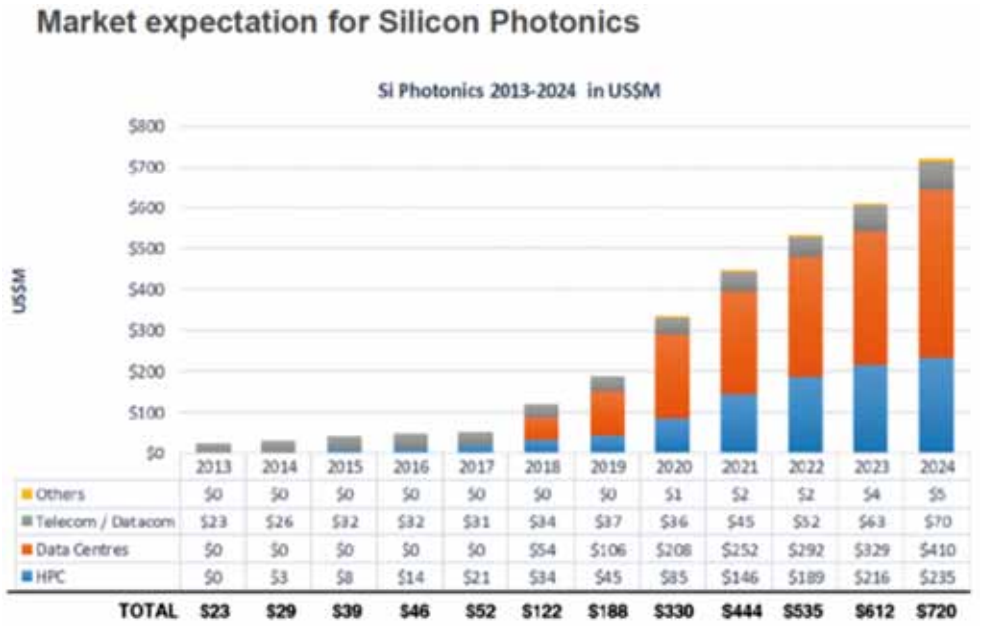


Fig. II.2.18: Short range Wireline market and technical specifications

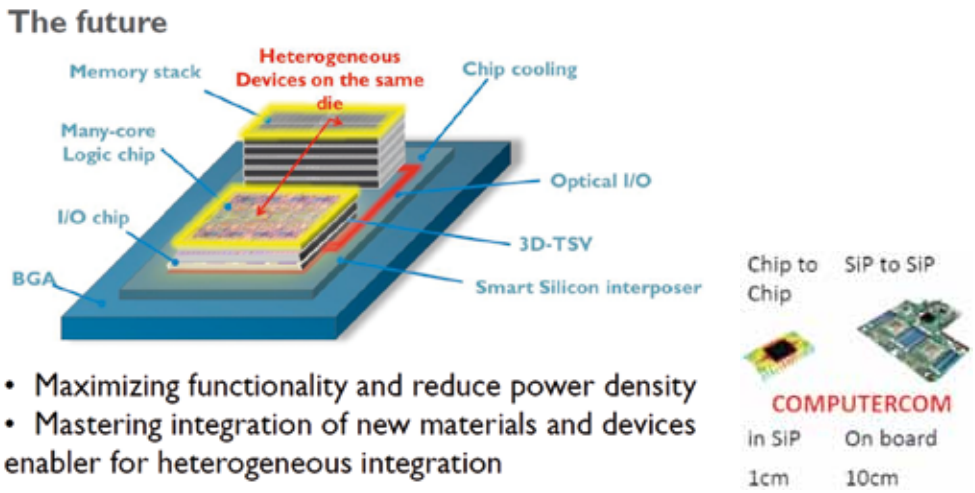


Fig. II.2.19: Short range Wireline Technology challenges

Main recommendations for technology research

Antennas & Passives

On demand re-configurable and tunable Antennas and Passives, very compact and massive MIMO antennas, with beamforming systems and very high antennas' directivity for all the used band, 0-6 GHz and mmW. Work may address metamaterials, NEMs, MEMs and integrated passives technologies, packaging and modules, design, systems and microsystems.

Transceivers & Front End Radio

High Data Rate

Up to 100 GHz and up to THz Transceivers, stable and accurate local oscillators, and antennas' interfaces targeting high and agile spectrum usage, with wider communication bands, allowing Full-duplex communications and solving Interference management, with on demand new PHY waveforms generation. Work may address new generation of nm CMOS, beyond CMOS, and mixed Silicon-III-V technologies, NEMs, MEMs, and new physics devices, combined with new design methodologies, modelisation and wireless long range, short range or wave guided systems.

Low Power Radio

Ultra-low power transceivers for WSN and IoT Networks, with µW consumed power objectives. Work may address Wake-Up Radio, Ultra-stable ultra-low power time reference, charge transfer, or time-frequency modelisation and design methodologies, CMOS, Beyond CMOS, NEMs MEMs, and new physics devices, wireless, including ultrasonic, or silk guided systems.

Wireline

Low cost 1300 nm and 1500 nm laser sources, optic modulators, LEDs, and PIN diodes, with their electrical interfaces, drivers and Trans impedance receivers, for modulations giving 400 Gbs to Tbs. Work may address photonics integrated components, including laser and VCSELs, copper wireline interfaces, 3D packaging methodology, Multiphysics modelisation and simulations, CMOS beyond CMOS, and low cost exotic More than Moore processes.

II.3 Smart Sensors

Executive summary

Global challenges for today's technology concern more sustainable, ICT-enabled strategies for healthcare, energy and environment. The role of edge-of-the cloud devices and of the generated big data are expected to drive the creation of new ecosystems and include 11% of the world economy by 2030.

The technology-Market developments[1] moved from a Processing Information "Moore" age (from the 80's to 2010) to a present Sensing Interaction in the "More than Moore" age (from 2010 to 2030, exploiting mobile computing and communication technologies). The expectations for the future are about an Actuating Transformation "Beyond Moore" age (beyond 2030, with smart cities & homes, autonomous vehicles and Industry 4.0 driving the application scenarios). This means that the technology is moving from simple sensing to smart sensing in almost every object, enabling new classes of services and applications.

The exercise of performing an European smart sensor roadmap is broad, complex and diversified because sensing technologies are very diverse and not driven just by scaling and costs, such was the case of CMOS. The exponential growth of the importance of smart sensors was first pointed out in Europe and worldwide by the FET Flagship initiative Guardian Angels for a Smarter Life in 2011, a project that build roadmaps for energy efficient smart sensors in a perspective of 10 years. Only later some industries came with roadmaps for the so called 'Trillion of sensors planet'. This means that Europe played a pioneering role in understanding and predicting the importance of smart sensors to support edge of the cloud applications in the future economy.

Among many domains for smart sensor applications, NEREID has chosen to focus on two main fields: (i) healthcare and (ii) automotive, as application drivers. These two fields have a high relevance for the European industry and research.

In the healthcare sector European countries are coming second after US, while in automotive, Europe excels in the autonomous vehicle market. Moreover, the European leadership in the automotive will be reinforced in the coming 5-10 years thanks to the presence of major technology manufacturers, early commercialization of automated vehicles and public organizations supporting the advancement of these vehicles[2]. In addition, most of the sensor types and challenges outside these fields are similar and relevant for industrial segments such as consumer electronics (MEMS accelerometers, magnetic, chemical and gyroscopes), industrial (image sensors), infrastructures (air quality gas sensors) and defense (LiDAR sensors).

Overall, connected objects (as part of Internet of Things, IoT), big data, software and algorithms, zero-power or self-powered sensors, sensor fusion, wireless sensor networks and system-in-package are all important topics for a more complete sensor roadmap.

1 Sensors for Wearable Electronics & Mobile Healthcare 2015 Report by Yole Development.

2 ADAS (Advanced Driver Assistance System) by systems and sensors, Global Opportunity Analysis and Industry Forecast, 2013 – 2020, May 2015, (www.alliedmarketresearch.com)

Relevance

Competitive value

The European automotive industry includes many world leaders and Europe is expected to lead the future autonomous cars market with the Advanced Driver Assistance Systems (ADAS) which predicts a worldwide market of 60 B$ by 2020[3]. On the other hand, European medical industry has a competitive position within the global market. European medical diagnostics and wearable market is the second highest revenue generator, owing to well-penetrated healthcare system and favorable regulatory policies[2].

Automotive sensors are enabling in major automotive scenarios involving less energy consumption (fuel-efficient and hybrid electric vehicles), less pollution (reduction for carbon footprint with stringent government laws and regulations towards vehicular emission) and improved safety and security of passengers (with autonomous cars and regulations to avoid road accidents). Progress in these domains is expected to boost the market growth and open new opportunities in the field of automotive sensors.

Improvements in healthcare sensor technology and required infrastructure will accelerate the extension and increase of its scientific excellence and competitiveness, which enable a cost effective fully sustainable healthcare system with truly personalized medicine, prevention and wellness for European citizens. This certainly will drive an economic benefit of healthcare costs.

This favorable position for European highly value added smart sensors and systems (proposed by ECSEL[3]) needs to be maintained and supported by massive investments of resources against the very competitive Asia-Pacific markets and other emerging countries. At the same time, these investments could activate a strong emergence of startups, the creation of bridges that improve the overlapping between the excellences of European technology offer (that it is often sold abroad, e.g. IMEC) and the European Industry (that buys their component from abroad) by forming a new sustainable ecosystem of European industries with high innovation content.

Societal benefits

Energy and environment, as mentioned above, are two present global challenges. The road transport research in Europe (ERTRAC) supported by EU policies have set out key ambitions[4]: (1) The European road transport sector should be 50% more efficient by 2030, (2) CO_2 emissions will reduce significantly (80% cars, 40% trucks) and new fuels will enter the market, and (3) transport schedules (mobility) will be 50% more reliable and traffic safety will improve significantly (reducing road accidents around 60% by 2030). Fuel-efficient hybrid electric vehicles is one of the path to reduce the carbon footprint and the energy needs of the society (if the energy is generated by renewable sources). Autonomous cars appear to improve x10 the safety of passengers and pedestrians while reducing fuel consumption by 10% and estimated cost of insurance by 30%[3].

In addition, there is an increase in the incidence of chronic diseases (cancer, cardiovascular diseases,

3 Smart Health, Smart Production, Smart Society (www.ecselju.eu/web/index.php).

4 European Roadmap Safe Road Transport, ERTRAC, June 2011 (www.ertrac.org).

diabetes) or of those coming from viral and bacterial infections (gastrointestinal, respiratory, sexually transmitted diseases, STDs or tuberculosis TBC). In 2011, approximately 5 million deaths occurred due to these diseases (AIDS, malaria & TBC). Awareness of health detrimental factors like obesity is rising as well as the population ageing (by 2025 more than 20% of Europeans will be 65 or older[1]). According to WHO (World Health Organization), cancer caused 8.8 million deaths in 2015, and is expected to reach 11 million by 2030[5]. The increase in these diseases will raise the demand for diagnostic devices (activity trackers, body monitors and multi-parameter real-time sensing) and for most of them, a low-cost, portable and fast diagnostic solution does not yet exist in the market yet. They could also serve to detect the incidence of health hazards caused by pollution. These emerging medical devices will also improve healthcare facilities (patient monitoring techniques from a distant location), treating these diseases in the emerging nations and simplifying the acceptance of personalized more-efficient medicine.

Vision

The Bosch scientist's vision for Automotive 2030+ foresees that the needs for cars in urban areas will also change. The carmakers have to re-think their business model and it will likely go mostly in the direction of "mobility-as-a-service" where the providers will offer electrical vehicles, car sharing, etc. All this is oriented to the "Last-Mile" micro-mobility as an attractive niche market where the car is intended to be used only for the last mile after public transportation (train, plane, etc.) because the classical motorized individual traffic will reach its peak. Future automotive sensors will serve as main drivers for the reduction of fuel consumption and car emissions, and to improve safety and security of the driver and other vulnerable road users. Government regulations combined with user needs will massively transform the automotive industry with a rapid market penetration of smart sensors and a mass adoption of Advanced Driver Assistance Systems (ADAS) amongst customers. Autonomous cars and drowsiness detection are one of the ultimate applications. It is predicted that the number of sensors per car will increase from 10 to 30 in the next 10 years.

The future growth of medical sensors is driven by personalized and preventive healthcare applications combined with healthy lifestyle electronic managers. New generations of non-invasive biological monitoring with embedded powering and sensing, multi-parameter sensing platforms, sensor fusion, wireless sensors networks (WSN), energy-efficient data processing, zero-power technological platforms or self-powered sensors, big data, energy-efficient data processing in cloud computing, etc. will predictably edge to the billion or trillion planet sensors of connected devices.

Scope and ambition

These roadmaps will cover medical and automotive applications and some specific selected sensors/categories as follows:

Automotive

- Sensor's for car internal system performance: Motion and Pressure sensor
- Advance Driver Assistance System (ADAS): Image, LiDAR and Infrared sensors
- Environmental monitoring: Gas and Particulate Matter sensors

Medical

- Physiological signal monitoring
- Implantable sensors
- Molecular diagnostics

Other sensor applications from other sectors are not specifically covered here. However, most of the sensors types and challenges covered in this document are similar and relevant for other industrial segments such as consumer electronics (MEMS accelerometers, magnetic, chemical and gyroscopes), industrial (image sensors), infrastructures (air quality gas sensors) and defense (LiDAR sensors). The choice in NEREID to focus on automotive and healthcare is considered that together can cover almost all the needs for a European roadmap on nanoelectronics devices and systems.

Main Concepts

A smart sensor is an electronic component that enables better control and monitoring of different operations, such as sensing physical inputs and produces a response by generating an output on a display or transmitting information in an electronic form for further processing using signal conditioning, embedded algorithms, and digital interface. Within this chapter

- Sensors for Automotive applications and
- Sensors for medical and healthcare

are considered, as characterized in the paragraph on scope and ambition on the left.

5 Fact sheets and World Cancer Report 2014 (www.who.int).

Sensors for Automotive applications

Automotive sensors are being widely used in four key applications; chassis, powertrains, body electronics and safety & security. Powertrain is the most popular application as sensors play an imperative role in improving fuel efficiency and reducing emissions. Most of the sensors used in automotive are shown below:

Common requirements for the sensor technologies in the automotive industry are:

- All the features (high resolution and contrast for the camera) guided by safety rules
- Capability to filter, process and evaluate big data, data safety and privacy
- Transferability to all vehicle types
- Robustness in all weather conditions
- Stability in large temperature ranges
- Redundancy for failsafe operation
- Long life-time, low power and low cost
- Capacity for data storage and a sufficient computing power
- Miniaturization
- High quality standards and performance optimization (resolution, form factor, etc.)

Sensors for navigation and car's basic system performance

MEMS devices are extensively used in cars for air bag sensors, electronic stability control, tire pressure monitoring, fuel injector pressure sensors, roll over detection sensors, vehicle dynamic control VDC sensors, throttle position sensors and other safety features.

Motion sensors serve to detect or track movement (in linear or rotational direction, namely accelerometer and gyroscope respectively) by monitoring a change in relative position of an object with respect to its surroundings and notify the users. There is an increased demand for accelerometers, gyroscopes and magnetometers. MEMS-based sensors have smallest form factor, which is a major reason for their faster adoption.

An optical position sensor detects the position of the targeted object. It detects changes in vehicle positions and provide parking assistance. In addition, these sensors ensure driver safety, thus releasing airbag depending on the position of the driver. A growth in adoption of these sensors is expected due to the increase demand of automobile safety and the rise of wearable medical devices adoption. Owing to their compact size, reliability, and low power consumption, high-performance and cost-efficiency of these sensors are being widely adopted with rising use in consumer electronics.

Proximity sensors detect the presence of an object of interest within the vicinity of the sensor. The function is featured with non-contact detection ensuring a high degree of reliability and durability of sensor.

Displacement sensors measure the displacement of objects of interest from one point to another. There is a growing popularity towards contact less sensing applications and the interest of automobile manufacturers towards the integration of sensor technology in automotive security and infotainment systems, as for parking sensor systems. Other non automotive applications are ground proximity warning systems, anti-aircraft warfare, roller coasters, conveyor systems, vibration monitoring systems, assembly line testing, mobile devices, etc.

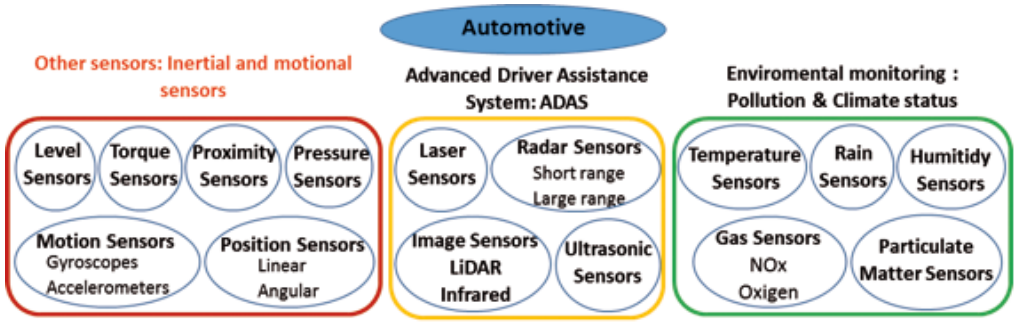


Fig. II.3.1: Class of Sensors in Automotive

Concept 1: Motion Sensors

Medium Term [+5 years] ●●●●●+

Long Term [+10 years] ●●●●●+

Key research questions/issues

- 3-axis accelerometers
- 3-axis gyroscopes
- IMU/ iNEMO SiP inertial modules (accelerometer, gyroscope, magnetometer)

Application needs & Impact for Europe

- Roll over detection for airbag
- Dead reckoning
- Anti-theft
- Pre-sage system
- Black box
- Infotainment
- Image stabilization in high-end Digital Still Cameras (DSCs)
- High-sensitivity tilt and security sensors
- Structural Health Monitoring (SHM) equipment
- Precision inclinometers in antenna-positioning mechanisms for communication

1 star = no critical, lower priority or unprovable to achieve it in this time-period
2 stars = Less critical, middle priority or less probable to come first
3 stars = critical, high priority or more probably to come first

Concept 1: Motion Sensors

Definition of FoMs or planned evolution

FoM / Planned Evolution	2023	2026	2029	2033
Price	< 4 $	< 3 $	< 2 $	< 1 $
Accuracy/Precision (over time and temperature)				
Stability (-40 °C to 105 °C) - Sensitivity changes, Offset drift	< 0.7 % - 0.4 mg/°C			
Acceleration (g) / Angular rate range (°/s)	±2 g, ±120 g / ±245°			
Full range	yes	yes	yes	yes
Measurement/response time?				
Form factor/miniaturization	< 3 x3 x1 mm^3	< 2x2x1 mm^3	< 1x1x1 mm^3	< 1x1x0.5 mm^3
Power consumption	< 15 µW	< 10 µW	< 5 µW	< 1 µW
Output data range / Bandwidth	0.5 -5 kHz			
Ultra-low noise	45 µg/√Hz			
Resolution	>10 bit	>12 bit	>14 bit	>16 bit
Non linearity	⁂		⁂	
Dynamic data batching	4 Kbytes			
Lifetime	10 years	12 years	15 years	20 years
Robustness, yield, repeatability	10000 g high sock suvivality	Extended T° -40°C – 180°C	20000 g high sock survivality	
Packaging – ECOPACK – green compliant	Ceramic, metal Open cavity LGA, Single die	Ceramic, metal Open cavity LGA, Multi die	Embedded die in laminate, Multi die	Fan-Out, WLP, Multi die
Calibration (recalibration requirements)	Minimal	Minimal	None	None

Technology Readiness Level (TRL) (design challenges)

Technologies	Medium Term	Long Term
MEMS (highest accuracy, stability, power consumption and miniaturization)	9 (5)	8-9

⁂ 1 star = no critical, lower priority or unprovable to achieve it in this time-period
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Competitive situation of Concept 1

MEMS devices are primarily driven by the automotive market. The Accelerometer and Gyroscope market is projected to reach $5 billion by 2022[6]. Parking sensor systems based on proximity and displacement sensors hold at present the maximum revenue share. Motion sensors are used in fully autonomous vehicles, in air bags, for voice-controlled equipment or across medical and healthcare sector (e.g. designing implantable medical devices) are expected to witness future growth opportunities in the European sensor market. On the other hand, accelerometer and gyroscope have become an integral part of all consumer electronic devices, although the MEMS market in mobile/portable applications grows more slowly than in previous years[6]. Major European companies operating in the motion sensors market are BOSCH Sensortec GmbH (Europe), STMicroelectronics, Safran, Colibrys SA (Germany), X-Fab and Atmel Corporation (Europe) among others.

Recommendations for Concept 1

Low accuracy of motion sensors restrains the market growth. MEMS sensors need to step up to the value chain, going beyond supply of components. Increase in automation for vehicles and low power consumption & small size are anticipated to provide numerous opportunities in the future. In addition, MEMS average selling price for consumer applications has fallen below $1, meaning that the use of sensors such as MEMS microphones, inertial, pressure and gas sensors in mobile phones has very low margins today. More lucrative industries or larger volumes are needed to boost MEMS market (automobile, defense & aeronautics, medical and industrial). Medical and automotive applications still offer pockets of growth and profitability as well as new opportunities. At present, the car industry uses on average 20 MEMS per car and autonomous cars will offer more possibilities for MEMS technologies. The Internet of Things (IoT) is growing fast and wearable electronics applications look very promising although volumes are not very high yet. In the future, more lucrative business will be mostly related to the data, the management and the services that this data could offer. The hardware could be given for free while the business will come from the services.

For portable applications and implantable devices, ultra low power is critical. The functional requirements of automotive include high value, high reliability and quality, and low price. However, a reduced power consumption (including the sensing and the data transmission) is very important.

Pressure sensor detects, measures, and transmits the information, which helps in analyzing the performance of a device. It monitors and controls the pressure of gases and liquids; and measures different types of pressures such as absolute, vacuum, gauge, and differential pressure.

Pressure sensors are the key components in reducing emissions and fuel consumption in emission control sensors, so as to decrease the air pollution. In addition, they are deployed for various safety concerns of passengers, such as Tire Pressure Monitoring Systems (TPMS), Advanced Driver Assistance Systems (ADAS), and Manifold Absolute Pressure Sensors (MAP). It also helps in deployment of air bags, throttle position, weight, sensing of passengers and Engine Gas Recirculation (EGR).

6 Accelerometer & Gyroscope Market (…) and Industry Vertical (Consumer Electronics, Automotive, Aerospace & Defense, Industrial, and Healthcare) - Global Opportunity Analysis and Industry Forecast, 2014 – 2022, February 2017, (www.alliedmarketresearch.com).

Concept 2: Pressure Sensors

Competitive situation of Concept 2

The global pressure sensor market is dominated by the automotive applications segment and together with the medical sector hold more than half of the total share. In addition, autonomous cars and the increase in demand of pressure sensors in medical applications will benefit automotive and medical manufactures to boost their market growth and increase their market share in the short-middle term (3-5 years).

Recommendations for Concept 2

Industrial and defence markets provide growing opportunities for high-end and high-margin devices such as inertial and pressure sensors. For consumer industry with smart phones and wearables has in turn pushed for smaller dies for integration in thinner handsets, reducing prices and shrinking margins. A shared manufacture infrastructure cost with other applications (e.g. between automotive and consumer), improved processes that further lower cost (like CMOS MEMS) or the creation of new devices with added value (e.g. software embedded within the sensor to deliver higher level functions) are some ways to limit the MEMS market regression.

Medium Term [+5 years] ●●●●●+

Long Term [+10 years] ●●●●●+●●●●●

Key research questions/issues

- Pressure sensors for automotive
- Pressure sensors for medical applications

Application needs & Impact for Europe

Automotive

- Tire Pressure Monitoring System
- Air Bag deployment
- Electronic Engine Control
- Idle stop
- Fuel Vapor
- Barometric Air Pressure (BAP)

Medical

- Blood pressure measurement
- Bladder examination
- Tactile sensors for fall detection
- Mass balance (to detect nanoparticles/atoms)

Automotive	Medium Term	Long Term
Side Crash detection	R&D and DP	Market Intro
Pedestrian impact detection	DP and RS	Market Intro
Seat Comfort System	R&D	Market Intro

1 star = no critical, lower priority or unprovable to achieve it in this time-period
2 stars = Less critical, middle priority or less probable to come first
3 stars = critical, high priority or more probably to come first
R&D = research and development
DP = Demonstration and Prototype
RS = Regulations and Standards
TRL = Technical Readiness Level
Market Intro = Market Introduction

FoM / Planned Evolution	2023	2026	2029	2033
Price	< 1.5 $	<1 $	< 0.75 $	< 0.5 $
Barometric Pressure Sensor	260 – 1260 hPa			
Pressure level precision	0.005 hPa		0.001 hPa	
Pressure relative accuracy	0.06 hPa		0.001 hPa	
Temperature accuracy	0.5 °C		0.1 °C	
Pressure temperature accuracy	0.5 Pa/K		0.1 Pa/K	
Stability				
Form factor/miniaturization	< 2 x2 x0.5 mm^3			
Measurement time	3 ms		< 1 ms	
Power consumption	5 µW	< 1 µW	< 0.5 µW	< 0.1 µW
Output power	8 dBm			
RF Transmitter/LC receiver	400 MHz / 300 KHz			
Lifetime	10 years	12 years	15 years	20 years
Robustness (-20, 200 °C), yield, repeatability	25000 g high shock survivality		⁂	
Packaging	Full molded		⁂	
Calibration				

Technology Readiness Level (TRL) (design challenges)

Technologies	Medium Term	Long Term
Piezoresistive	7-8	9
Capacitive MEMS (reduce manufacturing cost)	9 (5)	8-9
Optical	9	9
Electromagnetic	9	9
Resonant Solid state	7-8	

Advanced drive assistance systems (ADAS): sensors for autonomous cars

There is a major interest from technology providers to develop safer and more efficient transportation systems due to the persistence of road accidents. A majority of the manufacturers have indicated a keen interest in developing, manufacturing and commercializing driverless cars in the coming years. Today, ADAS facilitates safe driving and warns the driver if the system detects risks from the surrounding objects. Deployment of ADAS in vehicles enhances comfort along with compliance to government regulations for ensuring road safety. Main sensor types in ADAS systems are image devices (cameras, infrared and LiDAR sensors), radar sensors (short and large range), laser and ultrasonic sensors. Major ADAS systems based on those sensors are displayed below (apart from other dynamic systems as Tire pressure monitoring, adaptive front lighting or drowsiness monitor).

Vehicle cameras or image devices are mounted in and around a vehicle to provide real-time imaging and video recording of the inside and outside surroundings of the vehicle. These image devices offer various advantages such as 180-degree view of path for drivers, night vision, evidence in case of accident, and others. Advancement and fusion of technologies and equipment are likely to transform and increase the camera efficiency. It is categorized by 3D cameras (for gesture recognition, presence detection and driver monitoring), vision cameras (blind-spot side view, rear parking assistance, accident recorder, stereo cameras with direction and distance for LDWS and traffic sign recognition), LiDAR (light detection and ranging) sensors (for 3D mapping of surroundings) and night vision cameras (for pedestrian and animal detection).

Image sensors
are being integrated directly to central monitoring systems to allow automated response. Their use in autonomous cars will increase exponentially. Image sensors are classified into charge-coupled device (CCD) and complementary metal - oxide semiconductor (CMOS). Other applications are in medical imaging for 3D scanning, 3D rendering, image reconstruction or 3D modeling gesture recognition apart from traditional digital camera and camera modules consumer markets.

Light Detection and Ranging (LiDAR)
is a dynamically emerging technology which is used over conventional surveying methods to make the detection, examination and 3D mapping of geospatial surfaces easier and to provide highly accurate range data (improved resolution and data processing) in a shorter time than conventional methods. A LiDAR forms the image of the environment by scanning a laser and capturing the reflected light to compute distances. Novel LiDAR technology is micro-size, all silicon and low-cost, which allows its use for all kinds of new applications, including autonomous driving. However, LiDAR systems are still more expensive than other technologies (radars) due to the large number of components required: laser scanners, position and navigation system, high-resolution 3D cameras, photodetectors and MEMS.

Infrared detectors
detect infrared radiation, can measure heat and detect motion. Infrared detectors convert infrared radiation into electrical signals and are used in defense systems, medical and automotive applications (non-contact temperature sensing, infrared gas analysis, flame detection, temperature control systems, detection of human presence, and infrared spectroscopy).

Recent developments have manufactured highly sensitive infrared detectors at affordable prices. They are compact in size and have the ability to detect infrared light from long distances. However, they detect infrared images based on the temperature variations of objects (no differences in objects with a very similar temperature range). Their main present challenges are the higher cost (due to the required additional semiconductor components for increased sensitivity, the cooling techniques and the installation) and the inaccuracy in certain conditions (clean environment without dust and low humidity are required).

Fig. II.3.3: ADAS Sensoring vehicles

Images Devices for autonomous cars

Key research questions/issues

Technologies	Medium Term	Long Term
Image Sensors	Improve sensitivity, with smaller pixel size Flicker-free & HDR n-cabin NearIR Global Shutter	New sensing layer to replace Silicon Local computer vision Global Shutter/flicker-free/HDR Secured data links
LiDAR	Increase resolution	Higher integration into a small module
Thermal Infrared Sensors	Increase resolution	Cost Data fusion with CMOS imaging sensor

Application needs & Impact for Europe

Image Sensors	Medium Term	Long Term
Adaptive Cruise Control (ACC)	Standard function	Mandatory function
Lane departure Warning System (LDWS)	Standard function	Mandatory function
Park Assistance (PA)	Standard function	Mandatory function
Collision warning	Market Introduction	Premium class
Dynamic lighting	R&D and RS	Market introduction
Pedestrian detection	DP and RS	Market introduction
Traffic signal recognition	R&D and RS	DP
e-Mirror (interior and exterior)	Market Introduction	Standard function
Driver Monitoring	Market introduction	Standard function

LiDAR	Medium Term	Long Term
Automatic emergency braking (AEB)	RS and DP	Market Introduction
3D Mapping of surrounding	Market introduction	Premium class

Thermal Infrared Sensors – Night Vision Camera	Medium Term	Long Term
Night vision camera	Premium class	Standard function
Pedestrian/Animal detection	DP and RS	Market introduction

Technology and design challenges

Image Sensors	Medium Term	Long Term
Charge-coupled device (CCD)	Fully replaced by CMOS	Fully replaced by CMOS
Complementary metal - oxide semiconductor (CMOS)	⁂	⁂
Single-phonon avalanche diode (SPAD)	Higher integration with 3D stacking, Pixel size decrease	Both Time-of-Flight and Image within the same SPAD sensor
3D hybrid stack backside illumination (BSI)	Market Introduction	Standard function

Technology and design challenges

LiDAR Component
- Laser scanner
- Position and navigation systems (GPS/GNSS)
- 3D cameras (as before)
- Photodetectors (solid-state as Si avalanche photodiode)
- MEMS

Thermal Infrared Sensors – Night Vision Camera
- Pyroelectric
- Thermopiles
- Thermodiodes
- Microbolometers

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Definition of FoMs or planned evolution (1)

FoM / Planned Evolution Image Sensors	2023	2026	2029	2033
ADAS domain control	Multifunction camera Sensor fusion Feet-off	Hands-off	Eyes-off	Mind-off?
(3D) Image Sensors				2033
Sensitivity			⁂	⁂
Price	5 $ to 10 $	5 $ to 10 $	5 $ to 10 $	5 $ to 10 $
N° of sensors/car	5	6	8	10
Autofocus (AF)			No AF in car	
Optical Image Stabilization (OIS)	No OIS in car		Market introduction?	
Dual camera technology	Standard function		Replaced by single camera with Lidar?	
Time of flight (ToF)	⁂			⁂
Structure light (SL)	Market introduction (in-cabin)		Standard Function (in-cabin)	
3D Sensing cameras/4D	⁂		⁂	
Saturation Signal	⁂		⁂	
Dark signal	⁂		⁂	
Resolution (pixel, p)	⁂		⁂	
Pixel size/Number	~3.5 um 2 Mp to 8 Mp		~2 to 2.5 um 4 Mp to 16 Mp	
Read noise	⁂		⁂	
Detection Range (m)	1–100 m	1–150 m	1–200 m	1–250 m
Field of view	60°	90°	120°	180°
Chip/Image size	3.5 um/ 2 to 8 Mp	3 um/ 2 to 10Mp	2.5 um/ 3 to 12 Mp	2 um/ 4 to 16Mp

Image Devices for autonomous cars

Definition of FoMs or planned evolution (2)

LiDAR				
Resolution	⁂			***
Price	< 250 $	< 200 $	< 150 $	< 100 $
N° of sensors/car	1	1	2	2–4
Power consumption				
Detection Range/ range accuracy	1-100 m / < 2 cm	1-150 m / < 1 cm	1-200 m/< 0.5cm	1-250 m/<0.1 cm
Scanning angle/ angular accuracy	270° /5–10°	300 ° /4–8°	330° /3–7°	360° / 2–5°
Scanning time	20 Hz	50 Hz	75 Hz	100 Hz
Thermal Infrared Sensors				
Camera resolution	⁂			***
Price	< 500 $	< 400 $	< 300 $	< 250 $
N° of sensors/car	1	1	2	3
Power consumption				
Pixel pitch/Number			100 um/ 82 x 62	
Detection Range (NIR/LWIR)	150 / 400 m	160 / 425 m	180 / 475 m	200 / 500 m
NETD (f/1; 300k; 50 Hz)				
Frame rate	⁂		⁂	⁂
Size/weight	⁂		⁂	⁂
Common features				
Failsafe			Mandatory	Mandatory
Robustness; Operating T° (-40 °C, 105 °C)			Mandatory	Mandatory
Reliability - Lifetime	10 years	12 years	14 years	>15 years

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Competitive situation of Image Devices for autonomous cars

Apart from the exponential increase in the use of image devices predicted for autonomous cars applications, there is a continuous market in mobile applications and an increased demand for better and sophisticated healthcare facilities, advanced resolution and visualization of accurate test diagnosis. Thus, 3D healthcare industry is anticipated to witness high adoption of 3D imaging and dominate the global market share by 2022. The CMOS image sensor (CIS) market with new functions and industries (medical, security, industrial, etc.) could reach $18.8B by 2011 (See Footnote 2 on page 40). European key players include Infineon Technologies, STMicroelectronics and Siemens Healthcare among others.

Recommendations for Image Devices for autonomous cars

Competition in image sensors will remain relatively open and can become a market opportunity for Europe as long as the growth pattern is maintained and key technology changes occur almost every other year. The ADAS trend is further increasing pressure on vendors to provide sensors beyond their current technical capabilities. Image analysis is the new frontier and early usage of artificial intelligence for many different industries. Finally, technologies as time of flight (ToF) is bringing device miniaturization and structured light (SL) is resulting in high-resolution mapping at reasonable cost. For the case of infrared imagers, the high cost of the technology has restrained the use of microbolometer to niche/ medium volume applications but this is changing which will allow the way to consumer applications.

Radar Sensors (Long range/ medium-short range)

Key research questions/issues

Technologies	Medium Term	Long Term
Long Range Radar (LRR)	⁂	⁂
Medium/Short Range Radar	⁂	⁂

Application needs & Impact for Europe

Long Range Radar	Medium Term	Long Term
Adaptive Cruise Control (ACC)	Standard function	Mandatory function
Emergency Brake Assistance (EBA)	RS and DP	Market Introduction
Collision avoidance or Mitigation (CM)	Market Introduction	Premium class
Pedestrian Detection	DP and RS	Market introduction

Short/Medium Range Radar	Medium Term	Long Term
Rear Collision warning	Market introduction	Premium class
Blind Spot Detection (BSD)	RS and DP	In Market
Cross Traffic Alert	R&D and RS	DP
Lane change assist (LCA)	R&D and RS	DP

Technology and design challenges

Technology	Medium Term	Long Term
Silicon	⁂	⁂
Silicon Germanium	⁂	⁂

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TRL = Technical Readiness Level
Market Intro = Market Introduction

Radar sensors provides long- and mid-range functionality, which allow automotive systems to monitor the environment around the vehicle to help prevent crashes. A radar is an object-detection system where the radio waves are used to determine the range, angle or velocity of objects. They are less unaffected by adverse weather conditions and pollution (as infrared detectors) and they have 360° sensing.

Competitive situation of Radars Sensors

There are regular upgrades in the ADAS technology, which facilitate competitiveness in the market. In addition, the increasing awareness on safety and safety regulation as the same time as an increasing demand for comfort driving and multifunctional system help the market to growth. In the following figures, the sensor modules and functions for autonomous cars and market share shows a high increase for in the cameras for surround, long and short-range radars and the ultra sound sensors (Yole developments reports[2]). In addition, the ADAS evolution will pass firstly for the introduction of multifunction cameras, then the sensor fusion and finally a highly automated driving assistance based on fusion of comprehensive environment information.

Key players in Europe are split among automotive suppliers as Robert Bosch, NXP or Infineon and manufacturers as Peugeot-Citroen SA, Jaguar Cars limited and Fiat-FCA among others.

Definition of FoMs or planned evolution

FoM / Planned Evolution	2023	2026	2029	2033
Long range Radar				
Distance of object recognition	250 m			
Price	100 $	80 $	60 $	50 $
N° of sensors/car	1	1	2	2
Frequencies	79-81 GHz			
Short range Radar				
Distance of object recognition	0.2-30 m			
Price	30 $	25 $	20 $	10 $
N° of sensors/car	4	5	5	6
Frequencies	24-77 GHz			
Common Radar sensors features				
Failsafe	⁂		⁂	
Efficiency	⁂		⁂	
Noise level	⁂		⁂	
Robustness (-40 °C to 125 °C)	⁂		⁂	
Reliability - Lifetime	10 years		15 years	
Packaging	⁂		⁂	

Recommendations for Radar Sensors

The general challenges from the automotive markets cover the technology and packaging, a full eco-system ("from transistor to housing") which include the multi-domain co-design (chip, package, system) and the reliability (see WP5 Roadmap too). In addition, the necessary building blocks for monitoring an autonomous car includes not only sensors but also software, Electronic Control Unit (ECU), data management, GPS and connectivity which require interaction among WPs.

Pollution/Air quality (Environmental) monitoring based on gas sensors

Pollutants released from vehicles (automobiles and powered vehicles, industries, power plants diesel generators, etc.) into the environment can be controlled by setting up emission standards, which dictate the limits of pollutants such as CO_2, NO_x and SO_x. Low emission vehicles are fully electrical or hybrid, which involves a combination of traditional engines (Internal Combustion Engines), and electric vehicles in order to reduce both pollution (low emission batteries) and the dependence on oil.

In addition, Gas sensors and Particulate Matter detection are very demanding for other applications specially to measure the Indoor/outdoor Air Quality and see the influence on our health (in combination with physiological signals monitoring). It exists a common air quality index in Europe CAQI[7] based in three major pollutants: particulate matter (PM 10), nitrogen dioxide (NO_2) and ground-level ozone (O_3). When data also available three additional pollutants are also take into account: particulate matter PM 2.5, carbon monoxide (CO) and sulfur dioxide (SO_2).

7 http://www.airqualitynow.eu

The Figures of Merit (FoM) from the following table has been considered for the most demanding application, as portable gas sensor where the size, form factor and power consumption are crucial FoMs which would not be the case for the gas sensors on cars.

Key research questions/issues

Technologies	Medium Term	Long Term
Gas Sensors	⁂	⁂
Particulate Matter Detection	⁂	⁂

Application needs & Impact for Europe

Gas Sensors	Medium Term	Long Term
CO, SO_2, NO_2, O_3 (IAQ: indoor/outdoor, vehicle emissions)	R&D, RS and DP	Market introduction

Automotive fuel cell	Medium Term	Long Term
Blood alcohol content (BAC)	Market Introduction	Market Introduction

Medical diagnostic (Asthma or odor detection)	Medium Term	Long Term
Toxic, explosive, fire or injurious gases (industrial, infrastructure)	R&D, RS and DP	Market introduction

Particulate Matter Detection	Medium Term	Long Term
PM 2.5	R&D, RS and DP	Market introduction
PM 10	R&D, RS and DP	Market introduction

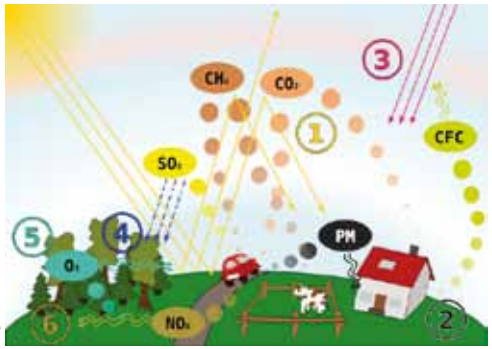

Fig. II.3.3: Enviromental Sensprs

⁂ 1 star = no critical, lower priority or unprovable to achieve it in this time-period
⁂ 2 stars = Less critical, middle priority or less probable to come first
⁂ 3 stars = critical, high priority or more probably to come first
R&D = research and development
DP = Demonstration and Prototype
RS = Regulations and Standards
TRL = Technical Readiness Level
Market Intro = Market Introduction

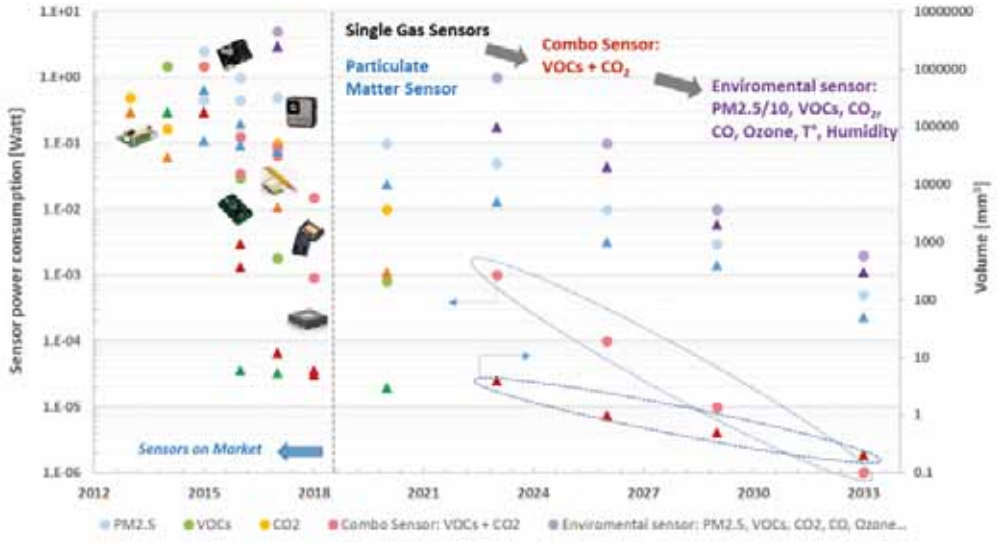

Fig. II.3.4: Gas Sensor classification and roadmap

Pollution/Air quality (Environmental) monitoring based on gas sensors

Technology and design challenges

Technology	Medium Term	Long Term
Metal oxide semiconductor (MOS)		
Nanometal oxides – Resistive MOX-CMOS		
MEMS Micro-hotplates MOS	First products in Market	First products in Market
Electrochemical Sensors	In Market Large size (2 cm), limited life-time (< 2 years), mature	In Market
Solid-state CMOS imagers	DP High power consumption ~50 mWatt, poor sensitivity	DP
Polymer sensing layers (possible with MEMS resonating layers)	R&D	R&D
Carbon-based (SW-CNTs)	R&D and DP	R&D and DP
Moisture Absorbing Material	Low cost and suitable for mass production (+)	Humidity monitoring
Spectroscopy	Few in market	
Optical IR sensors (non-dispersive IR: pulsed emitter and detectors)	In Market	In Market
Chromatography	High sensitivity but high cost and size	Typical laboratory analysis
Quantum dots, nanotubes and nanowires	R&D Low TRL (2-3), Integration challenges	R&D

Competitive situation of Gas Sensors

The growing awareness of air pollution will be driving the demand for gas sensors. The environmental gas sensor market is expected to grow over $3 billion by 2027[8] including indoor, portable and fixed outdoor air quality. The gas sensor market is dominated by US, Europe occupies a second position and the Asia-Pacific region is expected to grow at the highest CAGR margin (the bubbles sizes in the figure below represent the market size of the individual countries).

Recommendations for Gas Sensors

Emission standards that dictate the limits of pollutants such as CO_2, NO_x and SO_x, released from vehicles and industries into the environment, need to be stablished.

Low emission vehicles as hybrid ones, which involve a combination of traditional engines and electric vehicles will further reduce the pollution (low emission batteries) and the dependence on oil.

Pros and Cons

Pros	Cons	Target gases and/or application field
Metal oxide semiconductor (MOS)		
Low cost High sensitivity (but poor at room T°) Wide range of gases	High T° operation Long recovery time Structural instability High power consumption	Industrial application and civil use
Nanometal oxides – Resistive MOX-CMOS		
Longest lifetime 5-10 years Fast Stabilization time	Large size High cost High power consumption Need of calibration	
MEMS Micro-hotplates MOS		
Small footprint Low cost Ultra-low power consumption	Limited by sensitivity	Mobile market
Polymer sensing layers (possible with MEMS resonating layers)		
High sensitivity at room T° Short response times Low energy consumption Low cost	Long-time instability Irreversibility Poor selectivity	Portable applications Indoor air monitoring Workplace like chemical industries
Carbon-based (SW-CNTs)		
Ultra-sensitive Great adsorptive capacity Short response times Low cost, weight and simple Large surface/volume ration Good corrosion resistance	Lack of CNT growth control Variability Hysteresis Low TRL	Detection of partial discharge (PD)
Spectroscopy		
High sensitivity, selectivity and stability Long lifetime Short response time	High cost	Enable on-line real time detection
Optical IR sensors (non-dispersive IR: pulsed emitter and detectors)		
Highest accuracy High sensitivity, selectivity and stability Longest lifetime Enable miniaturization (MEMS)	Large size (not for mobiles) High power consumption (~150 mWatt) High cost Inaccuracy in certain conditions	Remote air quality monitoring Gas leak detection systems with high accuracy and safety High-end market applications

8 Enviromental Gas Sensors 2017-2027, IdTechEx, (http://idtechex.com/research/reports/enviromental-gas-sensors-2017-2027-000-500.asp).

Pollution/Air quality (Environmental) monitoring based on gas sensors

Definition of FoMs or planned evolution

FoM / Planned Evolution	2023	2026	2029	2033
Gas sensors Technical Requirements				
Sensitivity (high ppb, medium/low ppm)	< 100 ppm		< 10 ppm	
Response Time	<0.1 s (A.D.)		Ms (A.D.)	
Sensor element power consumption	< 200 nWatt	<100 nWatt	<50 nWatt	<10 nWatt
Energy consumption (including the read-out circuitry)	< 100 µWatt	<50 µ Watt	< 10 µWatt	< 1 µWatt
Adsorptive capacity				
Sample rate (fs= 2x B bandwidth)	>0.1 KS/s		>1 KS/s	
Input full scale (FS)				
Normalized output signal (NS)			1%	
Resolution (Effective number of bits ENOB, N)	8		10	
Energy entire sensor readout	<100 fJ		<10 fJ	
Particulate PM 2.5 Technical requirements				
Sensitivity (high ppb, medium/low ppm)	50 µg/m3		1 µg/m3	
Response Time	5 min	2 min	1 min	30 s
Sensor element power consumption	< 100 µWatt	<50 µ Watt	< 10 µWatt	< 5 µWatt
Sample rate (fs= 2x B bandwidth)	>0.1 KS/s		>1 KS/s	
Input full scale (FS)				
Normalized output signal			1%	
Resolution (Effective number of bits ENOB, N)	1		2	
Other requirements				
Selectivity	⁂		⁂	
Reversibility				
Stability (accuracy)	⁂		⁂	
Auto calibration	⁂		⁂	
Reliability - Lifetime	5 years	7 years	10 years	12 years
Package Size (for mobile application)	< 3 cm^2		< 1 cm^2	
Form factor	⁂		⁂	
Integration (hybrid, 3D, on flex)	⁂		⁂	
Wireless/Wired connectivity	⁂		⁂	
Robustness (harsh environment)	⁂		⁂	
Business Requirements				
Price	2 $	1 $	< 1$	0.1 $
Volume (low, medium, high)	High		high	
Market evolution	Emerging	Niche	Growing	Mature

Sensors for medical and healthcare applications

The domain of smart health is developing very fast. Recent research trends in IoT-based health include network architectures and platforms, new services and applications, interoperability, and security aspects[9]. In addition, policies and guidelines are needed for deploying the IoT technology in the medical field. The potential of the sensors technologies for healthcare originates in the expectations to have them in the future as key components of the healthcare cycle[10]. A revolution in human model development is now possible by leveraging data from omics analyses, medical and imaging data, environmental and life style big data that are continuously updated by a multitude of biosensors at an unprecedented scale. Wearables will help to create disruptive advances related to smart micro/nano-systems, nanomedicine, and safer and more effective personalized drugs. The introduction of standards for privacy and security of healthcare data is crucial to enhance the market adoption as well as other policies and guideline to accelerate the procedure of FDA credentials.

Their main applications are: (i) remote patient monitoring (including disease monitoring, drug development and clinical operation and workflow optimization), (ii) home healthcare and, (iii) sport, fitness and wellness monitoring. The end-users for such applications includes healthcare providers, patients and active people, healthcare payers, research laboratories of pharma, biotech companies and government authority. Sensors for medical and healthcare applications are categorized here as: very small patches (on-body sensors), sewed into the garment (wearable sensors) or implanted under the skin (in-body sensors) implantable, wearable, and other

9 S.M. Islam et al., The Internet of Things for Health Care: A Comprehensive Survey, IEEE Access, volume 3, 2015, pp. 678-708.
10 A.M. Ionescu, presentation of CONVERGENCE Flag-Era project, Riga, 2017.

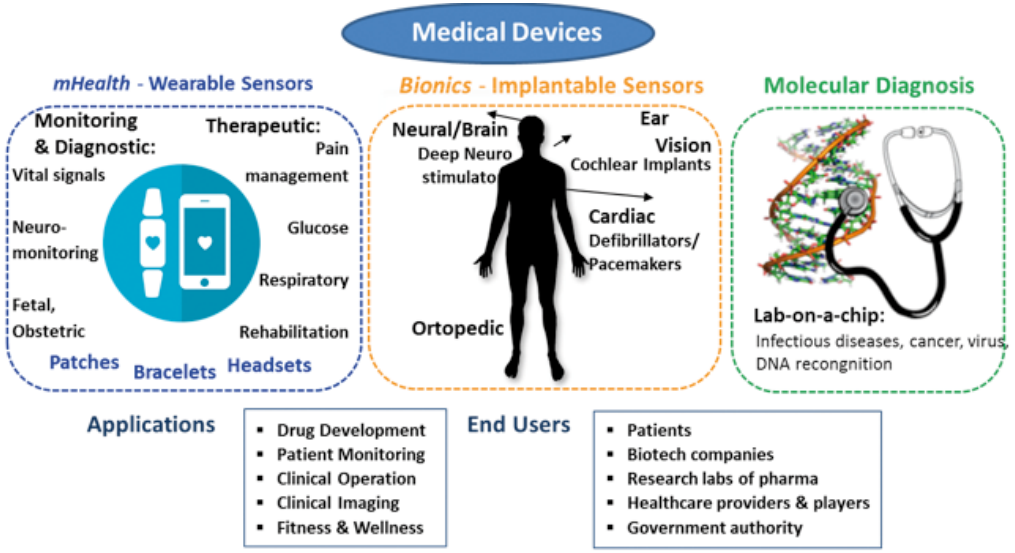

Fig. II.3.5: Classification of medical Sensors

sensors. The figure II.3.6 below depicts the concept proposed by the European Convergence Flag-Era project for an energy efficient wearable platform with embedded wireless low power bio- and environmental sensors and energy management for preventive life-style and healthcare, including feedback loops, and data processing locally and in the cloud.

The main challenges for medical wearables include to have: (i) a good signal quality that filters motion artifacts from the medical grades sensing (high accuracy); (ii) a frictionless technology with the right form factor and ideally non-contact sensing; (iii) a powerless wearable with high autonomy or ultra-low-power designs; (iv) biocompatibility; (v) a clinical validation with a large scale of clinical studies and trials; and (vi) a user adoption with the implies personalized algorithms and feedback. The future of medical wearables is related to edge of the cloud applications serving personalized and preventive healthcare approaches combined with healthy lifestyle electronic managers. Thus, these sensors which provide continuous health monitoring and real-time feedback to the user or medical personnel require also the integration into consumer-end devices and/or accessories.

Additional common requirements for sensors in the medical industry are:

- Safety/security
- Miniaturization, weight
- Manufacturability and cost
- Computing capacity and power
- Packaging and reliability
- Various sensing functionalities (genes, ADN, proteins, chemical species, position and orientation, interaction with ultrasound, with light, 3D surfaces, healthy or pathologic cells)
- Actuation: micro-pumps (drug delivery, micro-nano fluidics for biological samples analysis), movements (micro-robots, nano-particles), surgical tool control
- Energy harvesting and storage

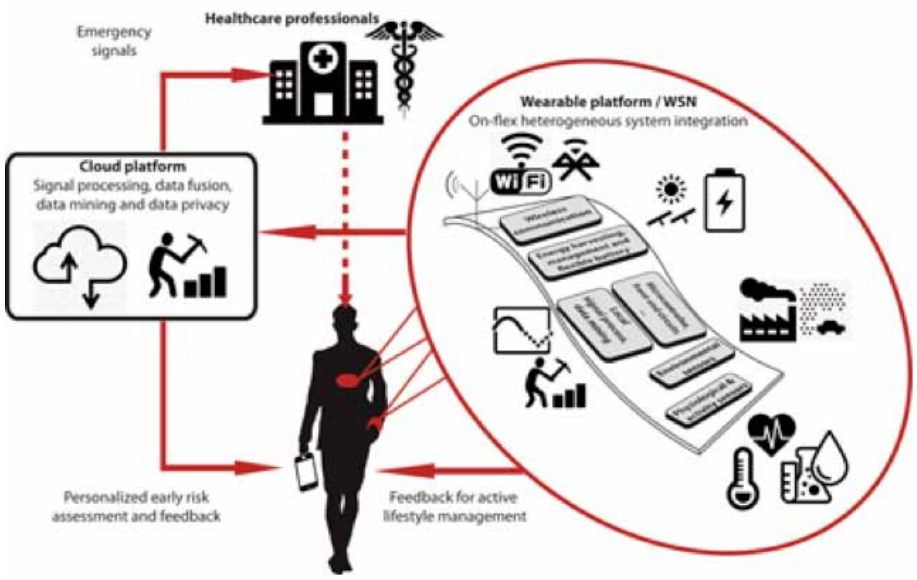

Fig. II.3.6: Concept of an energy efficient wearable platform

Physiological Signal Monitoring

Wearable medical device (including mobile-based medical devices), are defined as the devices with sensors attached to the body that detect and monitor changes in body signatures of various areas and organs like oxygen, glucose, insulin or cholesterol levels, heart diseases, blood pressure ingestion, pain relief, brain activity, hydration, temperature, quality, and quantity of sleep (apnea), calorie intake etc. Such biometric sensors embedded in the clothing's are called smart textile. Wearable medical devices feature wireless data transmission, real time feedback, alerting mechanism and have easy and timely sensing abilities. The data generated by wearable medical devices is analysed and further used by customers for a better health management.

There is a strong demand nowadays for the monitoring of the physiological signals to enhance the well-being through healthier life-style, to prevent cardiovascular accidents or dehydration while doing fitness and to improve the management of chronic/acute diseases. It can serve for diagnostic, monitoring, treatment and prevention of cardiovascular, diabetes, respiratory and neurological diseases or for wellness & healthcare system strengthened solutions. Cardiovascular diseases would expect to generate the highest revenue among them.

Medical grade wearable sensors can be inserted in headphones or glasses, carried on wrist (bands or watches) or on body (hats, socks or shoes) and as neck wear. Their use is expected to increase in the healthcare sector thanks to increasing trend towards IoT and owing to evolution in circuit miniaturization, low power microcontrollers, front-end amplification, and wireless data transmission. In digital health monitoring systems, wearable sensors facilitate continuous physiological access and reduce manual intervention.

Wearables are intended to be non-invasive and they can provide the monitoring of multiple parameters as

Monitoring and Diagnostic

- Vital sign monitors
  - Heart Rate Monitors (Chest-strat and wrist-based HRMs)
  - Activity Monitors
  - Cardiac Monitoring Devices
    - Electrocardiogram (ECG)
    - Implantable Loop Recorders (ILR)
    - Cardiac Output Monitoring (COM)
    - Event Monitors
  - Respiratory Monitoring Devices
    - Respiration rate
    - Capnographs
    - Anesthesia Monitors
    - Spirometers
    - Pulse Oximeters (heart rate, oxygen saturation)
  - Sleep Apnea Monitoring Devices
    - Sleep trackers
    - Wrist actigraphs
    - Polysomnographs
  - Hemodynamic Monitoring Devices
    - Blood Pressure
    - Blood Glucose
    - Cholesterol
    - Blood Gas & Electrolyte Analyzers/Monitors
  - Weight Monitoring Devices
  - Body and/or Skin Temperature Monitoring Devices
  - Skin conductivity (or perspiration) and heart sounds (phonocardiograph)
- Fetal, Neonatal and obstetric Monitoring Devices
  - Ultrasound
  - Electronic Fetal Monitoring devices (EFM)
  - Fetal Doppler

Physiological Signal Monitoring

- Neuromonitoring Devices
  - Electroencephalograph (EEG)
  - Electromyographs (EMG)
  - Magnetoencephalograph (MEG)
  - Intracranial Pressure Monitors (ICP)
  - Transcranial Dopplers (TCD)
  - Cerebral Oximeters

Therapeuthic

- Pain Management medical device
  - Neurostimulation
- Glucose/Insuline Monitoring
  - Insuline pumps
  - Other insuline monitor devices
- Respiratory Therapy
  - Ventilators
  - Positive Airway pressure (PAP, PAL)
  - Portable oxygen concentrators
- Rehabilitation devices
  - Accelerometers
  - Sensing devices
  - Ultrasound platforms
  - Spirometers

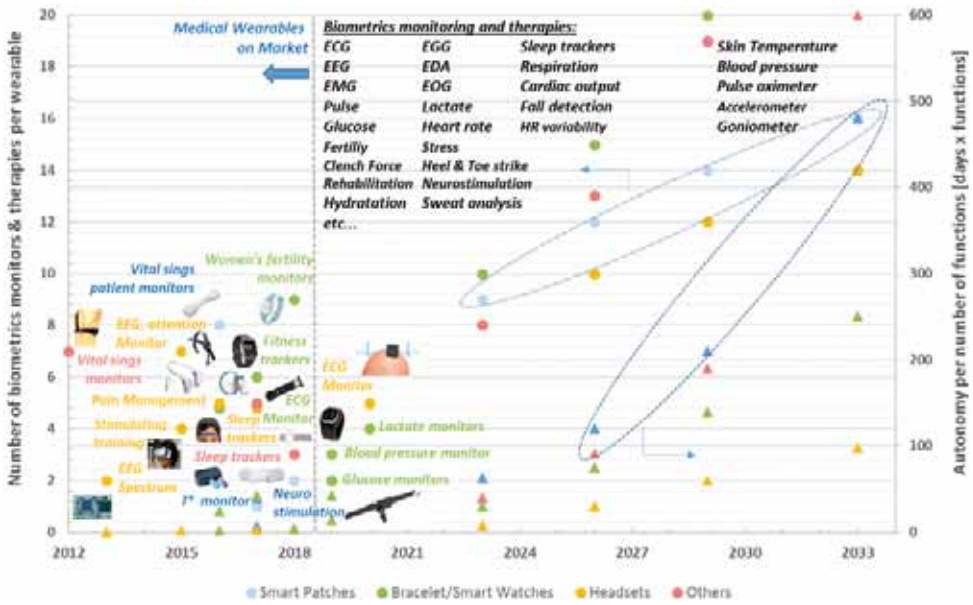

Fig. II.3.7: Roadmap on Biometrics Monitoring and Therapy

These sensors are more and more often combined in multiparameter monitoring devices and sometimes used to monitor remotely the patient for better and less invasive diagnostic as for: CRD (Cardiac rhythm disorder), CHF (Congestive health failure), ADD (Attention deficit disorder), ASD (Autism spectrum disorder), obstructive sleep apnea, TBI (Traumatic brain injury), dehydration, etc. However, as important as the data are the algorithms to analyze and interpret the information more efficiently, requiring personalization to the patient, like the delivered treatment. In addition, there is an essential role of clinical partners to drive applications, systems requirements and definitions of validation tests.

Physiological sensors serve also to detect the incidence of health hazards caused by pollution (air quality monitoring described later) and rising concerns about health and well-being. Moreover, the need for easy and convenient patient monitoring techniques from a distant location could fill this existing application gap.

Technology and design challenges

- Ions and/or biomarkers sensors
- Temperature sensors
- Pressure sensors

1 star = no critical, lower priority or unprovable to achieve it in this time-period
2 stars = Less critical, middle priority or less probable to come first
3 stars = critical, high priority or more probably to come first
R&D = research and development
DP = Demonstration and Prototype
RS = Regulations and Standards
TRL = Technical Readiness Level
Market Intro = Market Introduction

Medium Term [+5 years] ●●●●●+

Long Term [+10 years] ●●●●●+ / ●●●●●

Key research questions/issues

- Patient based devices
- Hospital based devices
- Driver impairment Monitoring

Application needs & Impact for Europe

Patient based

- Blood glucose meter
- Cardio meter (real time by a health patch)
- BP monitor
- EEG monitoring for epilepsy for children
- Activity monitor – Actimetry
- Fitness monitor (skin temperature, conductance, humidity, 3D accelerometer, ambient temperature with 100 h autonomy)
- Smart multifocal contact less for presbyopia
- Energy expenditure monitor (EE)
- Stress monitor

Hospital based

- Blood pressure meters & monitor (ECG, PPG)
- Vital signal monitoring
- Apnea & sleep monitor (including EEG, EOG, EMG)
- Pulse oximetry (neurological monitoring device)
- Congestive heart failure (tracking fluids instead of a thorax radiographny required)
- Chronic obstructive pulmonary disease
- Pregnancy contraction monitoring
- Dialysis

Driver Impairment Monitoring

- Alcohol-locking system
- Drowsiness mitigation systems
- Driver inattention

Physiological Signal Monitoring

Competitive situation of physiological signal monitoring

The top impacting factors for mHealth market are the cost and convenience (for the patient, the hospital, etc.). The technological innovations and integration of wireless technology in medical device is influencing faster adoption. The affordability of smartphones, government initiatives and increasing lifestyle diseases are secondary factors while the weak reimbursement coverage and the technological awareness among ageing population are not any more relevant in the medical industry. One of the key players in Europe is Philips Healthcare, but there are many European SME's and spinoffs in the medical sector than needs a further support to enter in the global market.

Recommandations for physiological signal monitoring

Medical devices development including market introduction is very difficult nowadays, related to the long and tedious development stage, followed by the high cost of clinical validations, and the difficult process of CE labelling / FDA approval in case of novel device concepts (non-standard validation tests). As a consequence, the total device development period ranges typical from 10 to 15 years, and is very expensive, often unaffordable for standards SMEs and spinoff companies. The creation of a European excellence consulting and advising clinical validation center would support the development of novel medical devices and reduce the time to market for them. For example, it would be very useful to standardize some metrology or validation tests for the hermeticity of advanced device package methods (i.e. based on polymers combined with ceramic diffusion barriers). Issues are also seen with respect to security and privacy of patients having e.g. implants with remote control. The availability of guidelines regarding prevention of hacking would be an important help for European institutes and companies developing smart implantable devices.

Definition of FoMs or planned evolution

FoM / Planned Evolution	2023	2026	2029	2033
Sensor element power consumption	< 200 nW	< 150 nW	< 100 nW	<50 nW
Sensing time	1 min	50 s.	40 s.	30 s.
Resolution	>8 bit	>9 bit	>10 bit	>12 bit
Multisensing	Activity parameters + a few biomarkers + air quality monitoring	Full activity + Tens of biomarkers + air quality monitoring	Full activity and energy expenditure + Tens of biomarkers + full environmental monitoring (air quality)	Full activity and energy expenditure + Hundreds of biomarkers + full environmental monitoring (allergens, pollens, etc.) + feedback for behavior engineering
Price for low cost medical patches / Price for smart sensing modules in wrist based devices	~5 Euro ~10's Euro	~2 Euro	~1 Euro ~10 Euro	Paid by subscription services
Non-invasive	Minimum invasion	Non-invasive	Fully non-invasive	Contact-less?
PCR-free			?	Yes
Portability	Yes			Yes, full flexible embedding
Lifetime	Hours to Days	Days to weeks	Weeks to months	Months to years
Certification and validation test procedure	Yes			Yes
Autocalibration	Yes			Yes

Bionics: Implantable Sensors

Bionics also known as biomedical implants are artificial addition to the body. These artificial implants mimic the function of the lost or non-functional natural organ such as limb or eye. Rise in geriatric population results in the upsurge in number of incidence of chronic disease such as hearing and vision loss, cardiac disorders and neural disorders, with an important decrease in quality of life and dramatic increase in medical costs as consequence. In parallel, increase in technological advancements such as most recent pacemakers or cochlear implants (with speech recognition features), led to higher adoption of medical bionics. However, high cost of these medical devices and corresponding medical treatment, as well as the stringent approval processes for medical devices are severe challenges, which hinder the market growth.

There are various domains for which the use of implantable sensors is considered very interesting (non-exhaustive list): vision (e.g. bionic eye), ear (e.g. cochlear or auditory brainstem implants), orthopedic (e.g. electrical bone growth stimulators), cardiac (e.g. pacemaker, artificial heart or heart valves, ventricular assist device), neural/brain (e.g. neurostimulators), etc. Not only medical implants but also devices in very close contact with body tissue are considered, such as smart contact lenses to restore vision.

Sensor devices used for medical implantations are based on a wide variety of technologies and working principles. In addition, some of them have been already described in other applications or concepts (such as the accelerometers). The implantable sensors roadmap table intends to cover the specificities, figures of merit, design challenges andKey research issues common to most of known bionics. No specific application is selected in this concept.

Bionics: implantable sensors

Key research questions/issues

Technologies	Medium Term	Long Term
Specificities of implantable sensors (figures of merit bellow)	Very critical to the final performance	
Validation tests and certifications (not defined by medical directives yet)	Difficult, expensive and time consuming	Certifications & validation tests defined by medical directives

Application needs & Impact for Europe

Application	Medium Term	Long Term
Vision	⁂	⁂
Ear	⁂	⁂
Orthopedic	⁂	⁂
Cardiac	⁂	⁂
Neural/brain	⁂	⁂

Technologies	Medium Term	Long Term
Novel hermetic package technologies based on flexible polymers (for miniaturization and biomimetic devices)	R&D phase	Packaging solutions available Power solutions for >10 cm implantation depth available
Wireless power supply (difficult when the sensor is deep in the body)	Induction allows only for implant depth of a few cm. Ultrasound and energy scavenging for deep implantation is in research phase	10-20 years (A.D.)
Long-term sensor sensitivity and stability	5 years (A.D)	5 years (A.D)

Deep Brain Neurostimulators

Cochlear Implants

Cardiac Defibrillators/ Pacemakers

Pulse oximeter

Insulin Pumps

Fig. II.3.8: Implantable Sensors: Bionics

Definition of FoMs or planned evolution

FoM / Planned Evolution	2023	2026	2029	2033
Form factor/size	Small, flexible	Biometric	Stretchable	Small, flexible, biomimetic
Biocompatibility	Yes	Yes	Yes	Yes
Biostability	Yes	Yes	Yes	Yes
Battery size	Small, flexible			No battery?
Tissue heating	Critical (related to the power consumption)			Controlled
Lifetime determine by the long-term sensitivity in order to avoid explantation	A.D. Not relevant for drug releasing devices			10-20 years (A.D.)
Autonomous sensors				
-Energy harvesting	Early research, only very limited energy can be harvested		R&D, only limited energy harvested but OK for devices with ultra-low power consumption	
-Remote/wireless power transmission	Replaced the transcutaneous cables Few cm implantation depth using induction.		Alternative power transmission methods such as ultrasound (for depth implants >10 cm)	
Wireless data communication and device control	Bi-directional/ Low data rate/ device control	Security and privacy		Communication between multiple implantable systems
Price (determined by local government, not by medical device manufacturer. Reimbursement by health insurance is important issue.)	Not very critical since the entire process is very expensive. (e.g. surgery, follow up in intensive care unit, etc.)			

Competitive situation of implantable sensors

Europe is well positioned for the medical market, as most of these sensor applications require extremely high reliability (failsafe devices) and a very accurate fabrication because the quality of the final product is very important. Although the cost of the final device is not unimportant, 'cheap fabrication' is not the rule, since quality and reliability is of utmost importance. The development of a medical implant is very difficult, since many scientific domains have to be combined. Highly educated scientists of many disciplines have to collaborate to fabricate a device with required quality, safety, and efficacy. Europe is ideally suited to perform such scientific work, since highly educated personnel is available, and since the cost requirements for an implanted medical device or more relaxed compared to quality requirements. An example of this fruitful multidisciplinary research is the recent application of motion sensors across the medical & healthcare sector, resulting in an interesting opportunity for future growth in the European sensor market as well as medical device market.

Recommendations for implantable sensors

The recommendations applied on physiological signal monitoring remain valid for this section.

Molecular Diagnostics

Molecular diagnostics technique is used to detect specific sequences in DNA or RNA, including single nucleotide polymorphism (SNP), deletions, rearrangements, insertions and for analyzing biological markers at the molecular level, such as genome and proteome; for diagnosis of the various infectious diseases, cancer, and other diseases/disorders; and to check the risk of genetic predisposition for a disease. Infectious disease diagnostic is an important application gap, owing to the increase in the number of patients suffering from viral and bacterial infections worldwide such as Human Immunodeficiency Virus (HIV), Hepatitis C virus (HCV), Human Papillomavirus (HPV), Chlamydia trachomatis/ Neisseria gonorrhoeae (CT/NG). Fast, simple and low-cost infection diagnostics directly at the patient bedside remains an unmet need in the health-care diagnostics market. Currently, rapid tests are available only for the simplest biological parameters (e.g. C-reactive protein, procalcitonin). For complex and life-threatening infectious illnesses however, reliable diagnostics can take place only through laborious and time-consuming procedures with the participation of a central laboratory employing qualified specialists.

Fig. II.3.9: Imagination of Molecular Diagnostic

The molecular diagnostic technology is categorized into polymerase chain reaction (PCR), hybridization, DNA sequencing, microarray, isothermal nucleic acid amplification technology (INAAT), and others (electrophoresis, mass spectroscopy, and flow cytometry). PCR contributed to the highest share in 2016, owing to the increase in usage in proteomics and genomics, which is highly cost-effective. Based on application, it is divided into infectious diseases, oncology, genetic testing, blood screening, and others (microbiology, neurological diseases, and cardiovascular diseases). End-users are hospitals, reference laboratories, blood banks, home health agencies and nursing homes.

The label free detection method is used for detecting biomolecules and their interactions. It is divided into cellular dielectric spectroscopy, bio-layer interferometry, surface plasmon resonance, optical waveguide grating technology and others. Within the products, there are biosensor chips and microplates. Specific applications related to label free detection are binding thermodynamics, binding kinetics, hit confirmation, lead generation and endogenous receptor detection.

Competitive situation of molecular diagnostics

Key player in the biomolecule diagnostic market includes Novartis AG, Siemens Healthcare GmbH, Roche Diagnostics and Bayer Healthcare among others.

Recommendations for molecular diagnostics

It addresses the need for better diagnostics and targeted therapeutic tools for physicians, athletes or patients (as dose reminder).

Medium Term [+5 years] ●●●●●+

Long Term [+10 years] ●●●●●+

Key research questions/issues

- Lab-on-a-chip

Application needs & Impact for Europe

- Infectious disease, cancer and other disorders medical diagnostic
- DNA probe/target recognition
- Single particle or virus detection
- Counting of particles/Particle trajectory tracking/Imaging
- Biological markers analyzer (e.g. acetone in breath for diabetes)
- m-RNA in blood (for cancerous tumours treatment efficiency)

Technologies	Medium Term	Long Term
CMOS Capacitive Sensor	DP	Market Intro?
Label-free based on FET SC NW	R&D	DP

Definition of FoMs or planned evolution

FoM / Planned Evolution	2023	2026	2029	2033
Number of parallel diagnostics	8	24	32	64
Lab-on-chip Response time	< 1 h			< 30 min
Sensitivity/detection limit	⁂			⁂
Price	6000 $		5000 $	Expensive but great cost effectiveness
PCR-free				Yes
Portability	Yes with external equipment			Fully portable
Power consumption/autonomy	⁂			⁂
Lifetime	⁂			⁂

Synergies with other topics

The synergies of all the concepts and interactions with other workpackages are common for all the described concepts and are summarized below.

Connected objects and Internet of things (IoT) – II.2 Connectivity

The connectivity technology is 2G, 3G, and 4G/LTE and can be integrated, embedded for navigation, telematics or infotainment applications. Fast connection to the wireless network and advanced infotainment systems are the two most prominent features. Connected cars facilitate connectivity on wheels offering comfort, performance, safety, and security combined with powerful network technology. In addition, this enables interconnectivity between two connected cars as the Machine-to-Machine (M2M) connectivity platform and numerous sensors and processors located in the car can provide accurate and real-time information to the driver.

⁂ 1 star = no critical, lower priority or unprovable to achieve it in this time-period
⁂ 2 stars = Less critical, middle priority or less probable to come first
⁂ 3 stars = critical, high priority or more probably to come first

Internet of things (IoT) is basically the networking of smart electronic devices or things to transmit data signals. It includes the devices, system & software and services. IoT technology will revolutionize the traditional paper-based healthcare treatment through simplifying access of real-time patient data and remote patient monitoring due to the growing demand for cost-effective treatment and disease management. This includes also the healthcare information technology (IT) infrastructure that intends to act as a bridge between all the medical entities and minimizes manual errors. Increasing exposure to smartphones along with 3G and 4G networks will further increase the use of mobile platforms in the healthcare systems (mHealth).

Zero-power or Self-powered Sensors – II.5 Power for Autonomous Systems

Energy efficiency per electronic function needs progress. The enabling zero-power approach will be disruptive overall for efficient autonomous systems. The combination of low power sensing and energy harvesting appears to be the most elegant solution. However, batteries implemented efficiency can extend sufficiently the lifetime of the device (5-10 years) and environmentally friendly printed batteries can be the solution for limited lifetime devices (few months).

Sensor Fusion and Wireless Sensor Network (WSN) – II.6 System Design

Multiparemeter sensing (as for medical diagnostics and healthcare monitoring), sensor fusion (as for the cameras in a car) are relevant applications that need to be study at system level including the network, the database (big data and security issues) and the analytics layer (algorithms).

WSN is a network of distributed autonomous sensors placed at a remote plant area, which uses the wireless technology to send signals or measurements to a control room thereby monitoring physical or environmental conditions. Battery enabled power is one of the main challenge to success.

Sensor packaging – II.6 Heterogeneous Integration

The packaging is considered as the most important feature to take into account in the sensor design and development (System in Package SiP versus System on Chip SoC). It is considered to be even more important than materials especially for bionic sensors and it make more sense for its optimization than the sensor itself. Close collaboration with WP5 is needed to create a specific sensor packaging road-mapping

Eco-system – II.7

A full eco-system ("from transistor to housing") which includes the multi-domain co-design (chip, package, system) and the reliability are general challenges from the automotive and health markets covering the technologies and packaging. Smart sensors manufacturing ecosystem in Europe is needed to avoid that the sensor market is monopolized by a few. With the design done by research institutes or universities, standard frontend and backend, control of wafer compatibility, secure shipping/ processing of wafers and high throughput at high quality is the way to success in the future.

Recommendations for Smart Sensors

General recommendations for the smart sensors in the automotive and in the medical/healthare segment described previously are the following one:

Shared manufacture infrastructure cost with other applications (e.g. between automotive and consumer), improved processes that further lower cost (like CMOS MEMS) or the creation of new devices with added value (e.g. software embedded within the sensor to deliver higher level functions) are some ways to improve margins as for example in MEMS market.

CMOS integration, compatibility and readout circuitry. New enabling technologies keep coming. However, integration becomes more challenging and reliability gets less predictable. It is predicted that smart sensors will remain as close as possible to CMOS standards.

Stability and reliability are the two most important features for the industrial take up of smart sensors. High reproducibility, ppb detection limits due to concentration, signature for functionalization, form factor and the power consumption of the platform are secondary characteristics that have to be taken into consideration for the sensor development. As mentioned already, selectivity is not the most important feature for sensing.

Regulations and guidelines are required to limit vehicle emissions and thus further reduce pollution and dependence on oil, to stablish emission standards that dictate the limits of pollutants (CO2, NOx, etc.) in indoor and outdoor air environments. Vehicle safety regulation are also a priority for Europe to reduce 50% of road accidents (cars, bicycles, pedestrian, etc.) by 2030. On the other hand, the different regulations and languages among national health organization are not helping to develop the medical market in Europe. Medical devices development including market introduction is very long (minimum 10 to 15 years), expensive and difficult nowadays, related to the long and tedious development stage, followed by the high cost of clinical validations, and the difficult process of CE labelling / FDA approval in case of novel device concepts (non-standard validation tests). The creation of a European excellence consulting and advising clinical validation center would support the development of novel medical devices and reduce the time to market for them.

Assembly testing, standards and metrology are crucial for the future success of smart sensors. There is a lack of metrology standards, commonly is difficult to interpret and it results in time consuming investigations.

Auto-calibrated, self-calibrated or an easy way of sensor calibration is not a common feature for the sensors in the market yet. However, this is highly interesting and required for future industrialization and a long-term sensor stability. As an example, CMOS capacitive sensors have the advantage that they do not need to be calibrated but it might have a poor sensitivity.

The maturity level of each sensor technology has to be assigned, estimating than a technology with a TRL higher than 6 would result to a product into market in less than 3 years approximately. The standards will be pushed very high in the different road-mapping but without excluding any technology for the next 10-year long term projection. The reason is that some application domains need mostly performance as in military while for others is the cost the most important factor or the repeatability, stability, reliability and yield for huge volume productions. A clear TRL correlation with technologies need to be stablished.

Thus, some of the smart sensor identified gaps by 2030 concern: manufacturability and cost (hybrid integration), low power consumption (energy efficiency), robustness of design and in production, and reliability.

II.4 Smart Energy

Executive summary

Power devices based on wide bandgap semiconductors (WBS) like GaN, SiC, Ga_2O_3, are poised to play an important role in future power electronics systems in addition to Si based workhorse technologies like IGBTs, Superjunction MOSFETs (e.g. CoolMOS), low/medium voltage MOSFETs (e.g. OptiMOS) and smart power BCD devices. WBS has a high breakdown strength and, in the case of GaN, allows for fabrication of high electron mobility lateral transistors, for which the electron mobility is not degraded as would be the case for traditional silicon MOSFETs. Together, these facts allow the fabrication of devices, which have orders of magnitude better trade-off between the specific on-resistance and the breakdown voltage. The roadmap for devices has been set up along four tracks, the first considers silicon-based devices, the second focuses on GaN based devices starting from materials towards integration, the third track is related to the evolution of SiC (again from materials to applications), and finally, future material systems (AlN, Diamond, Ga_2O_3) are considered which could offer benefits over the actual WBS in certain domains.

Relevance

Competitive value

Power Electronics is the technology associated with the efficient conversion, control and conditioning of electric energy from the source to the load. It is the enabling technology for the generation, distribution and efficient use of electrical energy. It is a cross-functional technology covering the very high Giga Watt (GW) power (e.g. in energy transmission lines) down to the very low milli-Watt (mW) power needed to operate a mobile phone. Many market segments such as domestic and office appliances, computer and communication, ventilation, air conditioning and lighting, factory automation and drives, traction, automotive and renewable energy, can potentially benefit from the application of power electronics technology. The ambitious goals of the European Union to reduce the energy consumption and CO_2 emissions can only be achieved by an extensive application and use of Power Electronics, as power electronics is the basic prerequisite for:

- Efficiently feeding-in wind and solar energy to the grids;
- The stabilization of power grids with fluctuating renewable energy sources;
- Highly efficient variable speed motor drives;
- Energy efficient and low-emission mobility with hybrid and full electric vehicles;
- An energy saving lighting technology;
- Efficient recovery of braking energy;
- Energy management of batteries;
- Control appliances and building management systems via the grid interface (smart grids).

Societal benefits

The estimated energy savings potential that can be achieved by introducing power electronics into systems is enormous, more than 25% of the current electricity consumption in the EU countries. Since power electronics is a key technology in achieving a sustainable energy society, the demand for power electronics solutions will show significant growth in the coming decades. European industry holds a strong position in the field of power semiconductors and modules and has established a wide band-gap semiconductors technology base. Europe also has high quality power electronics research groups at universities and research institutes with well-established networks and associations in Europe to provide platforms for discussion, cooperation and joint research. In addition, the European Union is funding many research and industrialization initiatives in the field of high efficient power electronics through the ENIAC, ECSEL and HORIZON 2020 program calls. On the other hand, outsourcing of research and technology to other countries (not only Japan, USA, but also emerging countries), strong research increment in these countries, and the possibility of key European companies being taken over by competitors from Asia, make it even more critical for Europe to keep up with the technological development. This requires continuous investments in research and development.

Vision

Smart Energy devices has the ambition to ensure the European technological capabilities needed for generating, distributing and consuming electrical energy and for replacing with electrical energy other sources like mechanical, hydraulic or combustion engines. The Smart Energy Task focus on the definition of the roadmap for technologies, materials, integration methodologies and processes for the realization of more efficient power management devices. Roadmaps for smart power need to cover different sectors:

- New highly efficient power devices based on wide band-gap semiconductor materials, like GaN on Silicon and later Diamond on Silicon or nanowire-based materials.
- New cost-efficient, Si based power devices to enable high efficiencies for mass-market applications
- Power management for very low power applications, as required for IoT, including the development of power scavenging technology.
- High temperature capable packages serving new materials and 3D technologies with lifetimes fulfilling highest requirements and the integration capabilities.

Scope and ambition

The Smart Energy devices roadmap will present the medium and long-term targets of the two main wide bandgap semiconductors, WBS, (SiC and GaN) as well as for the new promising WBS: Ga_2O_3, AlN, and Diamond. The aspects that will be covered within this roadmap are: i) materials and processing issues (including device architectures), ii) Applications, iii) Technology and design challenges; iv) Figures of Merit. In addition, important aspects of the roadmaps of corresponding Silicon technologies are presented.

Main Concepts

- Concept 1: Si based power devices
- Concept 2: GaN-devices and substrates
- Concept 3: SiC-based substrates
- Concept 4: Alternative Wide Bandgap Semiconductors

Concept 1: Si based power devices

Super-junction (SJ) devices

Silicon based power devices are rather mature from the semiconductor technology point of view. The material, reliability, and properties of Si/SiO_2 have been extensively researched and are well understood. Moreover, production capacities of 12" wafer diameter are already in place or are planned by various companies. Altogether, this maturity combined with the low area-specific resistance unit cost of super-junction (SJ) technology enables the power-conversion market dominance of these devices in various application segments. Further research in this field should grow (or at least preserve) the market share of European manufacturers in the competitive and cost sensitive SJ market. To achieve this, the main figure of merit to improve is Ron*A*cost. Which in turn can be optimized by further reducing the pitch of the SJ structure to achieve Ron*A values even below 5 Ohm*cm2 (currently 10 Ohm*cm2 is available on the market). Here, the main research paths are:

- Exploring the limits of trench-based and multi-epi/ multi-implant (ME/MI) based SJ technologies.
- Evaluation of alternative structuring concepts to trench or ME/MI.

It has to be noted that a further die size shrink (for a given Ron value) poses similar challenges and has the same relevance as for GaN and WBG devices regarding novel packaging concepts, thermal management, and understanding electrical parasitics, etc.

Competitive situation SJ

Currently, in the voltage range of 500-1000 V SJ-based devices dominate the power conversion market. Devices are used in both, hard- and soft-switching topologies for various applications and market segments like adapters, PC power, server/telecom, lighting, solar, EV-charging, eMobility, etc. There are several well-known manufacturers competing in these market segments.

- The European competitive position is as follows:
- Europe has a strong presence here, with manufacturers including: Infineon, STMicroelectronics…
- There are established competitors in the USA and Japan like Vishay, ON semiconductor, Toshiba or Fuji…
- China is catching up with a multitude of smaller companies supported by government and funding programs. Moreover, Chinese foundry HHGrace offers a power discrete fabrication services for the voltages 400-700 V.

Recommendations SJ

Due to its market dominance it is of utmost importance to continuously invest in the research and development of Si-based super-junction devices in order to grow/ preserve strong European presence in the 500-1000 V power-conversion markets. Besides the continuous reduction of the Ron*A*cost, in order to reduce variable product costs, also further growth of fully automated large scale 300 mm wafer production is necessary for cost reduction via economy of scale. Finally, R&D synergies, that are related to chip shrink, require further focus since these topics are also relevant for WBGs (i.e.: novel packaging concepts, heat management, etc.).

Insulated Gate Bipolar Transistor (IGBT)

Further development steps on Si-based IGBT technology are possible and crucial for future business success in the respective markets although this technology is mature and approaching their limits. The remaining improvement potential of Si-IGBT technology can be separated in four main categories:

Advanced Transistor Cell Design

Basic principle behind the design of advanced IGBT cell structures is to enhance the amount of charge carriers (holes and electrons) in the upper region of the device during the on state resulting in a low static on state voltage. This can be achieved by introducing sophisticated sub-µm mesa structures in between adjacent deep trenches (see Fig. II.4.1).

Vertical Design

In order to reduce static and dynamic losses a further reduction of device thickness is essential. The theoretical limits for Silicon are not yet reached. e.g. for a 1200 V device 110 µm to 115 µm are common and state of the art for high performance IGBT's whereas 80 µm to 90 µm are enough for the voltage blocking. Today's restrictions for further thickness reduction are given by critical application requirements like switching softness, cosmic ray robustness and thermal short circuit capability, where other specific measures will help to overcome these limitations (e.g. low inductance modules, field stop/p-emitter optimization, increased Zth).

Reverse Conducting IGBTs

The possibility of monolithically integration of IGBT and a freewheeling diode (FWD) in one device is demonstrated by several IGBT manufacturers. The so-called reverse conducting IGBT concept (RC-IGBT) enables a more efficient use of the given footprint in a power module and is therefore contributing to power density gain and cost reduction. The challenge is mainly to integrate technologically very differently optimized features (lifetime killing of diode, high p dose in IGBT cell) within one single die. Further device performance optimization is visible and full benefit of the concept is achievable by implementation of sophisticated gate driver concepts.

Increased Power Density

The fundamental development path of increasing power density is still valid and intact for IGBT technology as illustrated in Figure 2. Further steps in Si-IGBT technology are visible and essential for future business success. Increasing power density is leading to higher operation temperature (Tjop) and higher Tjmax of the device due to visible limitations in loss reduction. As a consequence, improvement measures for chip interconnect and chip packages are essential to prepare the path to increased device operation temperature. Beside measures of lowering Rth and improving thermal stability of package materials, a key roadmap target is therefore the improvement of power cycling capability in order to regain the desired product reliability. This leads to the necessity of the development of new chip metallization and interconnect schemes of highest power cycling capability. First development steps are done in the premium high power segment like Infineon's .XT technology with backside Ag sintering and Power-Cu front side metallization or double side cooling/sintering assembly techniques for electric drive train application. Next steps have to follow to improve cost effectiveness and roll out to the general purpose drive segment.

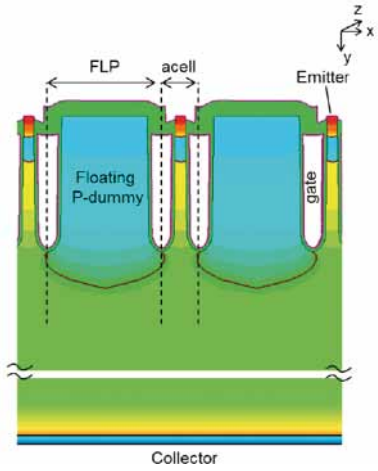

Fig. II.4.1: GBT structure with very small mesa
K. Eikyu, A. Sakai, H. Matsuura, Y. Nakazawa, Y. Akiyama, "On the Scaling Limit of the Si-IGBTs with Very Narrow Mesa Structure" in Proceedings of Int. Symp. Power Semiconductors and ICs, pp. 211-214, 2016.

Concept 1: Si based power devices

Key research questions/issues

IGBT, Advanced Cell Design	Short Term	Medium Term	Long Term
300mm substrate material	High resistivity material (>2 kV voltage class) cost	High resistivity material (>4 kV voltage class) cost	
Advanced sub-µm cell design	Switching control V_{cesat}-E_{off} trade-off First Gen. HV (>=3,3 kV) 2nd Gen. 1200 V, 1700 V	Switching control V_{cesat}-E_{off} trade-off 3rd Gen. 1200, 1700 V 2nd Gen. HV (>=3,3 kV)	
Vertical design	thickness reduction <110 µm (1200 V IGBT) Cosmic Ray Softness Thermal short circuit	Next level thickness reduction <100 µm (1200 V IGBT) Cosmic Ray Softness Thermal short circuit	
Precise wafer thinning	TTV 300 mm substrates	Next level TTV 300 mm substrates	
Interconnects, packaging, Tjmax	Reliability fs & bs interconnect Package/Housing materials Low stray inductance Harsh environment: Tjmax 175 °C cost	Reliability fs & bs interconnect Package/Housing materials Lowest stray inductance Harsh environment: Tjmax >175 °C cost	Reliability fs & bs interconnect Packgage/ Housing materials Lowest stray inductance Harsh environment: Tjmax 200 °C cost

Application needs & Impact for Europe

IGBT, Advanced Cell Design	Short Term	Medium Term	Long Term
Automotive EV/HEV (high power main converter)	Predominant (Si-IGBT) Prototype (SiC)	Predominant (Si-IGBT) Volume (SiC)	Volume (Si-IGBT) Predominant (SiC)
Automotive EV/HEV (charger)	Predominant (Si-IGBT) Volume (SiC)	Volume (Si-IGBT) Predominant (SiC)	Volume (Si-IGBT) Predominant (SiC)
Wind Power	Predominant (Si-IGBT)	Predominant (Si-IGBT) Prototype (SiC)	Predominant (Si-IGBT) Volume (SiC)
Motor drives (industrial)	Predominant (Si-IGBT)	Predominant (Si-IGBT)	Predominant (Si-IGBT)
Traction	Volume (Si-IGBT) Prototype (SiC)	Predominant (Si-IGBT) Volume (SiC)	Significant (Si-IGBT) Predominant (SiC)
HVDC	Predominant (Si-IGBT)	Predominant (Si-IGBT)	Predominant (Si-IGBT)

Technology and design challenges

	Short Term	Medium Term	Long Term
V_{cesat} * E_{off}	-25%	-45%	-60% (Si-IGBT limit)
Current density	+25%	+40%	+55% (Si-IGBT limit)

Competitive situation of IGBT

Si IGBT technology is not at its end of innovation roadmap. Further steps in the power density and the efficiency race are in progress. The gap to wide band gap transistors with respect to the most important economic parameter cost/power will get closer because of faster cost down on the wide band gap side. However, it's not yet clearly foreseeable if and when wide band gap semiconductor will reach the Si- IGBT benchmark. Nevertheless, wide band gap technologies will take over further market share in applications where high switching speed is possible, highest energy efficiency pays off and/or costs on system level can be reduced. For the next two decades a coexistence of Si-IGBT and wide band gap semiconductors is foreseeable in which a big part for Si-IGBT's will remain in the application areas of general purpose drives, large drives, wind power, traction and HVDC. Therefore further and extended development effort is necessary to defend the strong European position.

European competitive position:

- European Si-IGBT device manufacturers: Infineon, STMicroelectronics, ABB, Dynex, ON Semiconductors, …
- Packaging: All Si device manufacturers, Semikron, Danfoss, Bosch, etc.
- For Si-IGBT's, the position of Europe is still very good due to the strong position of Infineon as a chip manufacturer (300mm production line in Dresden and in Villach) and leading module suppliers (Infineon, Semikron, Danfoss, Conti).
- Japan is most competitive and partially taking over technology leadership position in packaging (Mitsubishi, Fuji, Hitachi)
- China is coming up extremely fast strongly pushed by government and funding programs

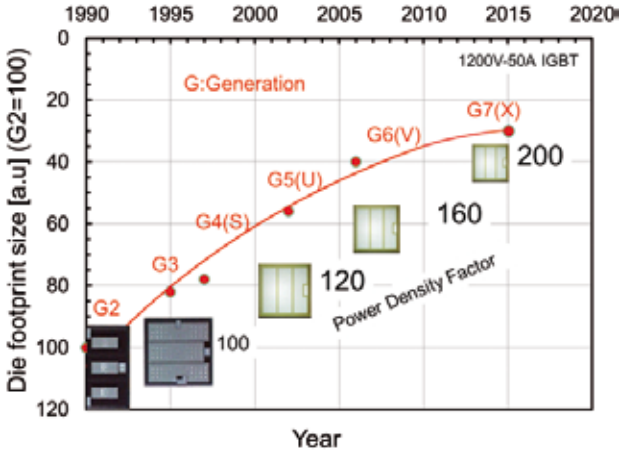

Fig. II.4.2: Chronology of IGBT chip size shrinkage and its power density (1200V IGBTs of vendor A)
N. Iwamuro and T. Laska, „IGBT History, State-of-the-Art, and Future Prospects," IEEE Trans. Electron Devices, vol.64, no. 3, pp.741-752, 2017.

Recommendations for IGBT

In the next decade further strengthening of the development of Si-IGBT technology is crucial to defend the strong European position in power electronics. Due to the fact that wide band gap semiconductors will take over only parts of the market, a very long coexistence of Si-based technologies with wide band gap is foreseeable over a long timeframe of at least two decades.

Fully automatized large scale 300 mm wafer production of Si-IGBT power technologies is still a key lever for cost reduction and competitiveness to Japan and Asia, especially the upcoming China. Further R&D efforts in this direction are recommended. From a technical point of view a strong focus has to be put on the optimization of the fine patterned trench cell, monolithically integration of IGBT and FWD (RC- IGBT) and vertical shrink of the device with highest accuracy. Additionally it is highly recommended to further enhance R&D efforts for advanced chip interconnect technologies (e.g. cost efficient sintering technologies) and advanced packages to enable higher device operation temperature and higher power density. The latter is fitting strongly together with major requirements coming from wide band gap technologies and therefore would pay off multiple times.

Smart Power BCD Technology Platform

Power IC market to integrate in a single silicon die multiple functions.

Thanks to the availability of a wide variety of elementary devices (Bipolar, CMOS, POWER Lateral DMOS and Passive) BCD products are present in almost all the current applications. During the last 30 years,

BCD platform evolution has followed with some delay the standard CMOS evolution. Clearly the very different applications covered by this flexible platform has been addressed with specific customization requiring dedicated device features for High Voltage applications (600 V and above) or specific Isolation capability addressed by fully dielectric isolated device built on Silicon On Insulator (SOI) substrates.

As for all the technology in the More than Moore arena, the evolution of this platform is driven by the application requirements and evolution:

- Digital Processing Capability increase.
  System miniaturization for Mobile applications together with some emerging applications in Automotive segment are pushing the migration to more dense technology nodes enabling the possibility to integrate in the IC a larger amount of logic together with an meaningful amount of Non Volatile Memory for code and data storage. The integration cost must be carefully evaluated and it may be alleviated thanks to the availability novel memory solution and larger diameter wafer.
- Power and High Voltage evolution.
  The continuous need of increased Electronic system power efficiency is requiring the integration of high performance Power device in BCD platform. Despite the lower level of power managed by a Power IC (due to package thermal limitations) the key power device target performance level requirement are not far from power discrete both in terms of conduction loss (RonXA) and in terms of Swicthing loss (RonXQg). Industrial applications (Industry 4.0) and Automotive Electrification are requiring Higher voltage devices drivers (1200 V) and high voltage galvanic isolation capability that will require specific process solutions in mature BCD technology platforms.
- Power Customization by Application.
  Specific technology modules are often key differentiator factors enabling optimum solution for specific applications. Power metal metallization is for example very important to manage in an optimum way the interaction between the silicon die and the assembly in the specific package family.

Within this scenario it's very difficult to identify a single parameter or set of parameters for the description of BCD technology evolution in the coming decade. Clearly the logic density capability, power device performance together with some new High voltage device rating need will be three key drivers for the evolution together with the function cost decrease.

Focusing on high voltage device performance, 40 V rated power device is a key component in all the BCD platforms addressing Industrial and automotive markets. Key performance parameter (Ron X Area) evolution is one of most important parameter for the STM BCD platform.

Keeping 20 % as target reduction for the new coming generation and assuming 5 year timeframe for each new BCD platform introduction the possible performance roadmap can be foreseen:

Year of Production	2020	2025	2030	2035
40 V Rated Integrated Power LDMOS Ron x A ($m\Omega*mm^2$) BV_{off} > 50 V	25	20	16	13

The above reported performance evolution level in an Integrated Smart Power technology platform has many challenges that need to be mentioned:

Recommendations for Smart Power BCD Technology Platform

Power device Safe Operating Area and reliability are today driving the major challenges for further performance improvement. Tailoring to specific mission profiles will most likely start to become very important in the future to secure power devices improvement.

Integration cost is a key factor to be carefully evaluated. In Smart power IC, Power stages are occupying a part of the total product area. Added process cost that may be needed to enable the performance improvement has to be carefully evaluated at global level to evaluate the impact on the product die cost.

Planar Isolated Architecture is today a must in Smart Power IC for the realization of multiple power topologies (Half Bridge, Full Bridges) together with driving circuitry often with different voltage class management.

Concept 2: GaN-devices and substrates

Substrate Diameter

Today, 6"–8" wafer size, low vertical leakage current, current collapse free GaN- on-Si wafers are available on the open market. Pricing for such material has come down significantly on the recent years. It is generally agreed that the magic cost target of 1.5 $/cm^2 for epitaxial material, which is also the price point at which GaN technology becomes cost-competitive with Si-based components at the device-level, can be achieved within the next couple of years under the important assumption that the wafers can be produced in volume. A next logical evolution would be to make the transition to 300mm wafer diameters, but it is as yet an open question whether this makes sense from an economical as well as technical perspective.

Voltage Rating

Standard products of GaN-on-Si typically feature an epilayer thickness of 4 µm to 6 µm, yielding a voltage handling capability of 650 V, including derating for temperature and lack of avalanche capability. Recent literature reports on boosted voltage rating of epi-wafers to values beyond 1200 V, by improvements in epitaxial recipes as well as increased layer thickness. However, due to the high intrinsic strain in GaN-on-Si layer stacks as well as the drive towards the adoption of semi standard substrate thicknesses, there is a fundamental limit to the maximal thickness (and breakdown voltage) that can be achieved.

Transport properties

The hetero-structures are typically based on AlGaN barrier material and have a sheet resistance of around 400 Ohm/sq (which directly influences the devices' on-state resistance). Future developments will see the sheet resistance reduced to values below 200 Ohm/sq. by adopting highly polarized AlN barriers or by using lattice matched InAlN barriers.

Vertical Devices

Besides lateral devices, also vertical devices are being investigated. They hold the promise of higher attainable power densities as well as avalanche capability, but they lack the benefit of electron transport along the 2-Dimensional Electron gas (2DEG). The vertical current flow makes this type of devices more sensitive to (vertical) threading dislocations, which pushes this technology towards growth on native GaN (or AlN) substrates. The latter are currently only available in small diameters and at a very high cost: significant progress on both aspects is required to make this a viable approach. An alternative track is possible to circumvent the high cost of bulk GaN substrates, which will need to come down significantly before devices can be produced economically. Growing GaN on foreign substrates (GaN-on-X), where X should be a substrate which provides lower cost, high quality GaN growth with higher quality and thicker buffers compared to what is currently possible on silicon.

On Chip Integration

A further path to cost reduction for GaN technology is to include several components on a single chip, allowing to save component, packaging and design costs for creating a full system. Beyond merely costs advantages, a monolithic integration will also enable the main potential of GaN to be tapped, which is a high commutation speed, leading to an increased switching frequency for the power circuit. Discrete Si power components can be quite readily integrated in a power circuit, however GaN components can deliver high power at a fast switching frequency. These properties lead to a stringent requirement on the design of circuit and interconnect parasitic. Integrating e.g. two switches on a single die can also significantly reduce interconnect parasitic, offering further system level performance benefits.

Key research questions/issues

	Short Term	Medium Term	Long Term
GaN-bulk Material	• Defect Density Quality • Wafer size, 6" • Cost	• Defect Density Quality • Wafer size, 8" • Cost	• Wafer size 8" • Cost
GaN-on-Si substrate	• Cost • Dislocation density • <1 E9/cm^2 • Deeper understanding of defects and their relation to reliability GaN thickness increase to 8 µm	• Wafer size scale up to 12" • Dislocation density • <1 E8/cm^2 GaN thickness • increase to 10 µm	• GaN thickness increase to 12 µm
Normally OFF devices	• Gate leakage Reliability • Avalanche & short circuit robustnes • Cost/die • Smart power GaN Monolithic integration HS/LS • Thin wafers Solderable interconnects	• Isolated gate device • Smart power GaN • Higher Vt • Scaling VBD • Ultra thin wafers	• Heterogeneous integration • Bipolar architectures • FinFET devices
Vertical devices	• Cost • Performance • Reliability • Gate dielectric Robustness • Thin wafers solderable interconnects	• Cost • Reliability • Performance scaling • Ultra thin wafers	• Bulk GaN • Bipolar architectures • FINFET devices

Application needs & Impact for Europe

IGBT, Advanced Cell Design	Short Term	Medium Term	Long Term
Low power DC/DC converter (POL)	Volume	Predominant	Predominant
Power supplies (PFC, e.g. for data centre)	Volume	Predominant	significant
Automotive EV/HEV (DC-DC converter, charger)	Prototype	Volume	Predominant
PV (roof/home)	Prototype	Volume	Predominant
Motor drives	Prototype	Volume	Predominant
Mobile chargers/adapters	Volume	Predominant	significant

Technology and design challenges

	Short Term	Medium Term	Long Term
GaN-on-Si substrate diameter	Cost Wafer size, 8"	Cost Wafer size, 8"	Cost Wafer size, 12"
GaN-on-Si substrate thickness	Semi std		
p-Gate architecture	p-Gate architecture dominant Blanket growth or blanket regrowth	Selective regrowth Polarization Engineering	Isolated architecture dominant
MIS-Gate structures	Solving basic material science issues	Dit engineering Industrialization	Reliability Yield
Ohmic contacts	<0.5 Ω.mm Alloyed metals	<0.2 Ω.mm Regrown contacts	<0.1 Ω.mm Regrown contacts
On-Chip Integration	Topology Reliability	Thermal management Packaging Cost	Cost System

	Short Term	Medium Term	Long Term
Thin wafers and interconnects	<100 µm	<60 µm	Electrically required thickness

Definition of FoMs or planned evolution

	Short Term	Medium Term	Long Term
R_{on} x A 100 V: 35 mΩ.mm² 600 V: 5 mΩ.cm² 900 V: commercially not existing	100 V: 17 mΩ·mm² 600 V: 2.5 mΩ·cm² 900 V: 7 m Ω·cm²	100 V: 9 mΩ·mm² 600 V: 1.2 mΩ·cm² 900 V: 4.5 mΩ·cm²	100 V: 5 mΩ·mm² 600 V: 0.6 mΩ·cm² 900 V: 2.8 mΩ·cm²
R_{on}·Q_g 100 V: 40 mΩ.nC 600 V: 400 mΩ.nC	100 V: 20 mΩ.nC 600 V: 200 mΩ.nC	100 V: 10 mΩ.nC 600 V: 100 mΩ.nC	100 V: 5 mΩ.nC 600 V: 50 mΩ.nC
R_{on}·Q_{oss} 100 V: 200 mΩ.nC 600 V: 4000 mΩ.nC	100 V: 100 mΩ.nC 600 V: 2000 mΩ.nC	100 V: 50 mΩ.nC 600 V: 1000 mΩ.nC	100 V: 25 mΩ.nC 600 V: 500 mΩ.nC
I_g	<1 µA/mm	<10 nA/mm	<1 nA/mm
V_{th} (at IDS 10 µA/mm)	>2.5 V	>3.5 V (tunable 1 V to 5 V)	>4 V (tunable 1 V to 5 V)
Lifetime (yrs @ Temp), Today: 15yrs (80% rated voltage), 1FIT	10 yrs @ 150 °C 20 yrs @ 125 °C 1ppm, 20 yrs (solar, automotive)	20 yrs @ 175 °C	20 yrs @ 200 °C
Short Circuit Robustness	5 µs @ 80% of V-rating	10 µs @ 80% of V- rating	

Other issues and challenges

	Short Term	Medium Term	Long Term
Parasitic (current collapse) over full V and T range	<10%	<5%	<2%
Reliability Today: <1FIT, 15 yrs (80% rated voltage)	Proven field failure rate <1FIT 1 ppm, 20 yrs (solar, automotive)	Proven field failure rate <1FIT 1 ppm, 20 yrs (solar, automotive)	

Competitive situation of GaN

GaN semiconductor devices provide a competitive advantage in terms of thermal performance, efficiency, weight and size. GaN is anticipated to be the next generation power semiconductor and thus different countries are indulged in developing widespread applications of GaN semiconductors. The wide band gap semiconductor technology has matured rapidly over several years. In fact, Gallium Nitride High Electron Mobility Transistors (GaN HEMTs) have been available as commercial off-the-shelf devices since 2005.

European competitive position:

- European GaN device manufacturer: Infineon, NXP, ON, Semiconductors, STMicroelectronics.
- For devices up to 650 V, the position of Europe is quite good and comparable to that of USA and Japan.
- Funding in Europe has become reasonable, however USA and japan did push much more money in the past.

Recommendations for GaN

One of the major restraints of the GaN semiconductor devices market is the high production cost of pure Gallium nitride as compared to Silicon carbide, which has been, in addition to mainstream Silicon, a dominant semiconductor material for high voltage power electronics for a decade. The various costs involved in the production of GaN devices include cost of substrate, fabrication, packaging, support electronics and development. Thus, high cost is one of the major challenges in the commercialization of GaN based devices. Though producing GaN in large volumes can help overcome these issues, currently, there is no widespread adopted method for growing GaN in bulk due to high operating pressures and temperatures, low material quality and limited scalability. It is therefore highly recommended to further enhance R&D efforts for improving GaN-on-Si epitaxy and corresponding devices with respect to quality, performance, and cost. This will be the all-important basis for a broad adoption of GaN devices in the power electronics market.

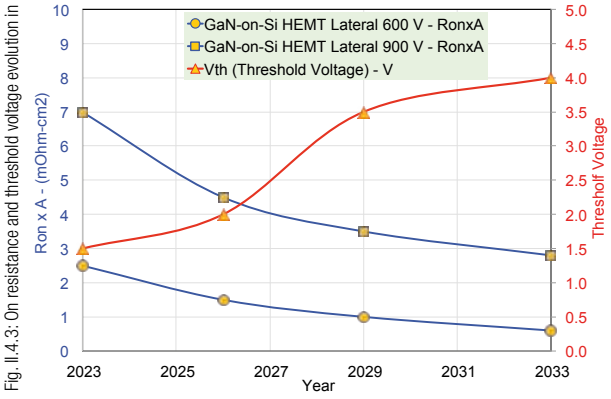

Fig. II.4.3: On resistance and threshold voltage evolution in GaN-based devices

Concept 3: SiC-based substrates

Power semiconductors are the key components of any power electronics circuit. Compared to the standard bulk Silicon, SiC has superior properties for the application in power electronics, i.e. higher breakdown voltage, lower losses as well as the capability for high frequency switching and high temperature operation. These performance data are related to important material's properties, e.g. higher energy bandgap, breakdown electric field, and thermal conductivity. The current maximum SiC wafer size in production is 150 mm.

Recently, SiC devices with breakdown voltages of 10 kV and higher have been developed for MV applications. This voltage rating noticeably surpasses that of commercial Si devices, such as 6.5 kV IGBTs. The breakdown voltage rating of this new device generation has not yet reached its limit. Latest SiC High Voltage (HV) power semiconductors, for example, MOSFETs, IGBTs, diodes and GTOs are presented that offer innovative opportunities for medium-voltage applications. These properties make SiC the ideal material for high current values (50A and higher) devices at high voltages.

Concept 3: SiC-based substrates

Key research questions/issues

Concept 2: SiCsubstrates and devices	Short Term	Medium Term	Long Term
EPI layers with low defect density, high homogeneity, and high growth rates	Enhanced growth rate	Life time defect engineering	Free standing p-Epi (removing entirely the substrate after Epi)
Trench power devices with high gate oxide reliability	Enhanced mobility Lower $R_{DS,on}$	Novel architectures	
High-voltage (>6.5 kV, 10 kV) Bipolar devices (e.g. n-IGBT, BiFET)	Bipolar degradation (interaction of recombination and stacking faults) ⇒ recombination engineering or ⇒ avoid stacking faults completely	Compensation devices	High performance n- IGBT
Solid state circuit breakers (relay replacement)	Low loss designs	High blocking voltages	
High-reliability power devices (exceptional lifetime, e.g. for aviation applications) and related driver circuits	Rugged design, low defects	Higher integration density	

Application needs & Impact for Europe

IGBT, Advanced Cell Design	Short Term	Medium Term	Long Term
Power supplies (PFC, e.g. for data centre)	Volume	Volume	significant
PV (roof/home)	Volume	Volume	Predominant
PV (MV, central)	Prototype	Volume	Predominant
Automotive EV/HEV (DC-DC converter, charger)	Prototype	Volume	significant
Automotive EV/HEV (traction inverter)		Prototype	Volume
Motor drives (industry)	Prototype	Volume	Predominant
Traction (trains, trams)	Prototype	Volume	Predominant
Wind power	Prototype	Volume	Predominant
Grid: power transmission and distribution (e.g. HVDC)		Prototype	Volume
Airplanes	Prototype	Prototype	Volume

Technology and design challenges

	Short Term	Medium Term	Long Term
Advanced passivation for high ruggedness (humidity, gases, environmental impacts)	In the substrate	On the chip	
Self-aligned process techniques for high manufacturability (e.g. TrenchMOS)	Prototype	Volume	
Wafer thinning and bonding Thermal, mechanical, electrical (Ron) Today: 100µm	50 µm	30 µm	Electrically required thickness

Definition of FoMs or planned evolution

	Short Term	Medium Term	Long Term
Ron	-20%	-40%	
Lifetime (yrs @ Temp)	10 yrs @ 175 °C	20 yrs @ 175 °C	
Gate charge	-25%	-50%	

Other issues and challenges

	Short Term	Medium Term	Long Term
Novel methods for accelerating life- time testing	On chips	On modules	
Novel reliability models	For chips	For modules	

Competitive situation

SiC is on the verge of market penetration for very high current values (50 A and above) and high voltages over 1000 V with the potential to allow for voltages far above 10 kV being the most advanced material. Next to the improvement of the device parameters and extending the limits, the appropriate integration of such advanced devices in new module architectures is of utmost importance to exploit all the benefits of the devices.

European competitive position:

- European SiC device manufacturer: Infineon, STM, ABB, Bosch, ON Semiconductors, etc.
- Packaging: All SiC device manufacturers, Semikron, Danfoss, etc.
- For devices up to 1700 V, the position of Europe is quite good and comparable to that of Japan. But, there are huge public funded projects in China and USA to catch up and especially in Japan and USA to take over the lead for voltage classes higher than 1700 V.
- China, Japan, USA have started the development of devices, Europe not really.

Recommendations

It is highly recommended to focus on the growth of thick epitaxial layers with low defect densities, e.g. very high current values (50 A and above), and high carrier lifetimes for high voltage devices, e.g. bipolar devices. To really deal with high voltages, the passivation on chip, e.g junction termination or advanced in chip passivation, as well as in the module for 3D integration has to be addressed.

Next to the costs and the yield of the SiC devices, the reliability issues have to be addressed. The current devices show a high robustness against high voltages and temperatures. But to derive adequate reliability and life time predictions, novel accelerating life-time testing and modelling of these devices have to be established. To exploit all the benefits of high current, high voltage devices, advanced 3D integration concepts have to be developed.

Besides GaN, a number of other wide-bandgap materials exist. The most cited is diamond that is considered to be the "ultimate material". However, technological obstacles (lack of efficient n-type doping, conductive surface channels and difficulties to make ohmic contacts) have for a long time blocked the demonstration of performant devices. Unless spectacular progress is made on these issues, no real-world implementations are foreseen and as such, diamond is not included in the roadmap. Besides SiC (for which a separate part of the roadmap is dedicated), we identify three major candidate materials: AlN, Ga_2O_3 and diamond.

AlN native substrate

Is probably the most interesting wide bandgap material, because it combines high thermal conductivity with a very large bandgap of 6.2 eV, higher than that of diamond. It can be easily combined with GaN-based materials to form heterojunctions (such as HEMTs). Currently few AlN bulk substrate suppliers exist (Hexatech, Crystal-N) and the substrates are 2" in diameter or below.

Gallium oxide

The latest kid in the block in wide bandgap materials is the Ga_2O_3. As it can be grown from the melt, it is potentially a low-cost material. It can be doped (with some difficulties) to make vertical devices and can be combined with Al_2O_3 as a gate dielectric. Recently, a number of publications reported on promising device characteristics. The major drawback is the material's low thermal conductivity. Ga_2O_3 is a material system, which allows processing devices with improved breakdown voltage compared to SiC and even GaN. However, the main advantage stems from the fact that the material can be grown from the melt and can thus be produced at very cheap rates when compared to GaN & SiC. However, the main disadvantage of this material is the very low thermal conductivity, which is a really undesirable property of power devices. Further research will have to demonstrate if devices can be fabricated, which can deal/overcome this issue.

Diamond

Is considered by many the ultimate material for fabricating power components. It has the highest breakdown strength of any known material, combined with an extremely high thermal conductivity. However, due to the wide bandgap it is also challenging to find a suitable dopant for diamond. Apart from this the growth of the material is also quite challenging. Initial demonstrator transistors are available in diamond, but much work will be needed to improve performance towards practical performance and demonstrate the capabilities of the material system.

Synergies/complementarities with other similar road-mapping activities

Several other road-mapping activities, related to wide bandgap semiconductors, have been started in the recent years, here we are listing the most relevant ones:

ECPE Roadmapping

The WBG Roadmap developed within the European Power Electronics Network (ECPE) has a strong focus on systems and applications searching for lead applications that can take advantage of the favourable properties of SiC and GaN on system level. The target applications for WBG power devices include automotive with the traction inverter, the DC/DC converter and on-board charger as well as PV inverters, industry drives in automation and robotics and grid-related applications for SiC in the medium or high voltage level. For these applications the main drivers for the use of wide bandgap devices are evaluated: the increase of power density regarding volume and weight reduction, the higher efficiency regarding the reduction of dynamic or static losses, the higher reliability, ruggedness and temperature capability as well as the easier controllability. In the next step the degree of market readiness and penetration was evaluated: demonstrator according to industry standards, first product available, significant market share and predominant market share.

PowerAmerica Strategic Roadmap for Next Generation Wide Bandgap Power Electronics

PowerAmerica aims to make wide bandgap (WBG) semiconductor technologies cost competitive with silicon (Si) based power electronics (PE), and to accelerate the adoption of silicon carbide (SiC) and gallium nitride (GaN) based components in markets and applications. PowerAmerica works to develop and implement well-planned but flexible strategies to accelerate this progress and facilitate collaboration across the PE community, including between end users and experts from prominent universities and government agencies. The PowerAmerica Strategic Roadmap outlines key markets and application areas for SiC and GaN PE, the performance targets GaN and SiC technologies are expected to meet over time, technical barriers to achieving those targets, and activities needed to overcome those barriers. The roadmap activities will guide strategic decisions for demonstrating the benefits of SiC and GaN, improving WBG semiconductor device performance, and increasing commercial use of SiC and GaN PE.

International Technology Roadmap for Wide Band-gap Power Semiconductor ITRW

The International Technology Roadmap for Wide Band-gap Power Semiconductors (ITRW) was co-initiated by IEEE PELS and organizations representing the USA, China, Japan, Europe, and UK in 2015. The International Technology Roadmap for Wide band-gap power semiconductor (ITRW) will provide reference, guidance and services to identify the future research and technology developments of wide band-gap power semiconductors and their application, and thereby provide a reliable and comprehensive view on the Strategic Research Agenda and Technology Roadmap.

Recommendations

Apart from WBG device development the WBG system integration is necessary to exploit the full potential.

- Packaging and system integration technologies enabling low parasitic inductances to master EMC issues
- Packaging and system integration technologies enabling reliability at higher temperatures
- Handling higher voltages on package/module level and system level: SiC in medium voltage (MV) applications e.g. in traction and industry
- Low inductance packaging and integration technologies: power PCB with chip embedding, system-in-package (SIP), switching cell in a package
- Passive components for fast switching: mainly inductors, reduce losses at high switching frequencies, thermal management of (integrated) passives
- Characterization, testing, modelling and reliability analysis of WBG packages, modules and converters

II.5 Energy for autonomous systems

Executive summary

As the communicating systems market is booming, the role of energy harvesting (EH) will be growing. Indeed, the number of connected devices is planned to increase by a huge factor of 200, while the number of mobile phones is just planned to increase by a factor 3. Connected devices are going to be used more and more in several fields such as healthcare, wearable, home automation, etc. The Internet of Things (IoT) market grows considerably leading also to the boom of the connected devices, and so highlighting the importance of energy needed to supply them in view of the limitations of current battery technology. In this particular case, we are focusing on small connected devices with low power consumption below a few mW (or even a few tens of µW).

Different wasted energy sources can be exploited and converted into electricity: sun or artificial light, heat, RF power (either intentionally transferred), mechanical movements and vibrations… Moreover this converted energy needs to be used and transferred wisely to sensors, microcontrollers or other electronic components included in the system. Thus power management circuits and energy storage devices become also an essential element.

In this roadmap report, we have assessed several promising technologies for EH and power management circuits including photovoltaic cells for outdoor/indoor light EH, thermal energy harvesting, mechanical EH based on three concepts: piezoelectric materials, electrostatic and electromagnetic energy conversion, RF energy harvesting/wireless power transfer and finally the power management circuits and microbatteries for energy storage.

Relevance and competitive value

Providing energetic autonomy to electronic devices will be a key factor in booming technologies like sensor networks and IoTs. This is true for applications with specific requirements, where a simple battery would not be sufficient, where using power cords increases largely the cost or complexity (i.e. avionics), or when the number of devices are so numerous that changing batteries could increase the maintenance cost. Other examples are in harsh environment were the electronic devices could not be reached/accessed easily, or in biomedical devices. The interest of the EH concept will be also to develop new devices compatible with silicon technologies for implementation in the fabrication line, which would attract the interest of semiconductor companies. New green solutions based on non-toxic and rare materials would be of high interest for the dissemination of energy harvesters.

Vision

Dissemination of energy autonomous electronic devices will only be possible if it is driven by applications. Actually the energy that can be generated from small EH devices is quite low with most of the technologies, but this could be sufficient for many sensing applications, knowing the fact that energy is in general randomly generated. In addition, research is progressing towards the development of micro-power architectures of application circuits. The evolution of the EH technologies will enable a growing number of possible applications and products to be placed on the market, which were unfeasible up to now. In the medium (>5 years) and long term (>10 years) roadmap of the covered technologies, we expect an increase on their performance or efficiency (more electrical energy produced for a given available energy). For the long term in particular, new materials (polymers, triboelectric materials, organic, perovskites…) and nanotechnologies will be used to obtain higher performances but also to replace toxic/rare materials used today (i.e. Bi_2Te_3 in thermal EH and lead based materials for piezoelectric conversion, rare earth based magnetic materials, e.g. NdFeB, for electromagnetic conversion). Energy storage for combination with the EH will require advances in storage capacity per unit footprint and power capability during device interrogation and transmission.

Power management circuits are expected to require lower input power (<100 nW), input voltage (<10 mV) and smaller surfaces (< mm^2) in the long term.

Scope and ambition

Targeting EH technologies with low fabrication cost, with high efficiency, and without toxic/rare materials is the main challenge. Adding flexibility and/or transparency is also an increasing demand for compatibility with wearables applications.

For the semiconductor companies, the interest is also to develop new devices compatible with Silicon technologies. The fabrication of components dedicated to energy harvesting and in particular to thermal energy is of high interest as no solution based on silicon technologies is available for implementation as of today.

Mechanical EH rely typically on input vibrations, and one of the main challenge is the compatibility with low frequency vibration source (most of applications use frequency vibrations <100 Hz) and the increase of the operational frequency bandwidth.

Although photovoltaic EH technology is mature (silicon based) for both outdoor/indoor applications, emerging materials are promising for their potential to add flexibility and low weight (thin films) at reduced cost and high efficiency (organics, dye sensitized, perovskites, etc.).

RF harvesting systems (referred as rectennas, rectifying antennas) have been widely used and studied in recent years due to the vast presence of RF sources in humanized environments. However, too low power densities have usually been experienced because of RF regulations and RF power transfer “on demand” solutions are currently preferred and are exploited in a large number of passive RF system applications, such as RFID, wearable or implantable devices, realized using eco-compatible materials.

Thin film solid-state solutions for energy storage have existed for some years now but more energy dense and higher power options at lower cost are required. Initial prospects to increase those may involve multilayer options and the use of thicker electrodes. New materials for both electrodes and electrolyte with increased conductivities will assist in meeting the targets. Nanostructuring and new printing capabilities are also of interest.

The main challenges associated to power management circuits are related to the miniaturization of the system embedding micro-transformers or power converters, the reduction of overall leakage enabling low power consumption and the development of energy-aware circuit design techniques.

Main Concepts

- Concept 1: Mechanical EH: Electrostatic transduction
- Concept 2: Mechanical EH: Piezoelectric transduction
- Concept 3: Mechanical EH: Electromagnetic transduction
- Concept 4: Thermal energy harvesting
- Concept 5: Photovoltaic Energy Harvesting
- Concept 6: RF energy harvesting/wireless power transfer
- Concept 7: Energy storage - Microbatteries
- Concept 8: Energy storage - Microcapacitors
- Concept 9: Micro-Power Management

Concept 1: Mechanical EH: Electrostatic transduction

The principle of operation relies on the use of mechanical forces to do work against the attraction of oppositely charged capacitor's plates; thus those generators can be considered as mechanically variable capacitors whose plates are vibrated by the movement of the vibration source. Typical structures include capacitor plates in form of fingers installed in central oscillating mass and in stationary comb. When the capacity is at its maximum value the electric charge stored in the capacitor is transferred to the external battery. To insure good capacitive coupling between oscillating mass and stationary comb the distance between fingers has to be as small as possible. In order to avoid the charging and discharging cycles, electrets (dielectric material with trapped electrical charges) can be implanted into one of the two parallel electrodes. This technology is a promising solution for CMOS-compatible, low cost, micro scale EHs. Most of the challenges will rely on the development of stable materials able to keep the electrical charges over many years and related to mechanical structures that can work in a large frequency bandwidth, in order to improve the harvested energy.

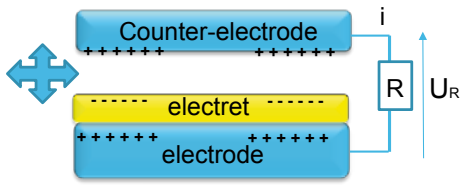

Fig. II.5.1: Cantilever-based electret energy harvesters

Competitive situation of concept 1

Among vibrational energy harvesters[1], the electrostatic transduction allows maximal miniaturization using MEMS technologies. Many proofs of concept devices have been presented at the scientific community but no industrial devices have been commercialized yet.

Recommendations for concept 1

- For vibration based harvesting, enlarge the frequency bandwidth (> 50 Hz) around low frequency target (below 100 Hz) is key to fit with applications.
- Develop dedicated power management circuits.
- Reliability of material is the key to maintain the charges over 10 years.
- Flexible and low cost approaches for wearable (body) applications should be developed.

1 S Boisseau, G Despesse, T Ricart, E Defay and A Sylvestre Published 31 August 2011 • IOP Publishing Ltd , Smart Materials and Structures, Volume 20, Number 10

Key research questions/issues

Technologies	Medium Term	Long Term
Improve efficiency with a reduced surface, volume	New materials: Fluorin polymers / surface texturation	Fluorin polymers / surface texturation
Increase input bandwidth, reduce working frequency for portable applications, adaptable devices	Non-linear mechanical systems for larger frequency bandwith > 30 Hz	> 100 Hz
Improve scalable technologies at low cost / related to efficiency -> but miniaturization reduce the energy	Higher energy density	
Increase reliability of integrated systems / stability vs time / keep polarization and charges > 10 years Increase performance of electret materials (charges leakage reduction)	Develop stable layers with time (polymers)	Encapsulated SiO_2 / triboelectric materials

Application needs & Impact for Europe

Technologies	Medium Term	Long Term
Industrial / Infrastructures monitoring for security (autonomous sensors) - on vibrating sources	Harvesting on pumps, industrial machines	
Develop wireless autonomous monitoring in transportation (car, planes…)	Harvesting on railway, train	Harvesting on cars, planes
Develop Wearable systems (electrostatic materials / triboelectricity) for human movement harvesting	Shoes	Medical patches

Technology and design challenges

Power Amplifier Technology challenges	Medium Term	Long Term
Develop low cost solutions and flexible approach to conform body	Optimized polymers	Low cost polymers
Develop tribolelectricity	Fluorin polymers / surface texturation	Low cost

Definition of FoMs or planned evolution

FoM / Planned Evolution	2023	2026	2029	2033
Volume power density (mW/cm^3) @1G[1] and 100 Hz	0.5 mW/cm^3	0.65	0.8	1 mW/cm^3
Volume energy per cycle[2] ($\mu J/cm^3$) @1G	5 $\mu J/cm^3$ per cycle	6.5	8	10 $\mu J/cm^3$ per cycle

1: G: input acceleration (1G = 9.81 m/s^2)
2: Cycle: 1 period of time defined by the given frequency

Other issues and challenges, interaction with other areas

- Power consumption of power management circuit
- Develop applications

Concept 2: Mechanical EH: Piezoelectric transduction

Most piezoelectric harvesters are based in a resonating device made of a cantilever beam, covered by a piezoelectric material and an inertial mass attached (see Fig. below), these devices are tuned to the characteristic mechanical vibration frequency of the application. As the cantilever is bent, strain is transferred to the piezo layer, which induces an asymmetric charge distribution, and therefore a voltage is generated. MEMS devices are very promising because their fabrication is CMOS compatible. Many companies exist actually exploiting this principle and integrating piezoelectric materials (mostly PZT, being toxic) on different substrates (metal foils, PCB…), very recently MEMS devices can be also found on the market by integrating AIN. Similar to the electrostatic concept, the main challenges rely on the increase of the resonance bandwidth, reduction of the working frequency to adapt to the applications, and increase of the energy generated per unit surface or volume.

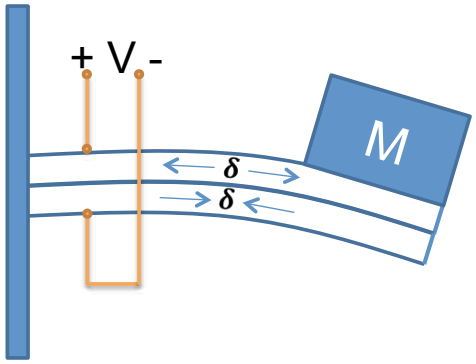

Fig. II.5.2: Classical structure of a piezoelectric energy harvester

Competitive situation of concept 2

Among vibrational energy harvesters[2], the piezoelectric transduction is one of the most exploited in research and at industrial level (MIDE, Smart Materials and Piezo Systems in USA, PI, CEDRAT, Smart Materials GmbH and ARVENI in Europe) thanks to its simple structure. It allows decent performance at small scales (~few cm^3 prototypes).

Recommendations for concept 2

- New sustainable materials should be considered to avoid lead based piezoelectric materials (i.e. AIN, ZnO, GaN and their composites, piezo-electret…)
- Develop micro and nano piezo-composites could be a key to improve devices performance.
- Develop new concepts leading to performance and bandwidth improvement at low frequency (e.g. frequency-up converters, hybrid, adaptable devices, exploiting non-linearities…).
- Device miniaturization and/or integrability on flexible substrates would a key to fit wearables and IoT applications.
- Packaging is also a key to improve performance and reliability, in particular at vacuum.

2 Larcher, L., Roy, S., Mallick, D., Podder, P., de Vittorio, M., Todaro, T., Guido, F., Bertacchini, A., Hinchet, R., Keraudy, J. and Ardila, G. (2014) Vibrational Energy Harvesting, in Beyond-CMOS Nanodevices 1 (ed F. Balestra), John Wiley & Sons, Inc., Hoboken, NJ, USA. doi: 10.1002/9781118984772.ch6)

Key research questions/issues

Technologies	Medium Term	Long Term
Improve efficiency with a reduced surface, volume	Develop packaging (Vacuum), integrate higher density seismic masses.	Small scale hybrid devices. Work on mechanical properties (fatigue strength, elasticity…)
Increase input bandwidth, reduce working frequency for portable applications, adaptable devices	Exploitation of non-linarites, frequency-up converting	Adaptable devices
Increase performance of piezoelectric materials	Porous materials	Nanotechnology, nanocomposites

Application needs & Impact for Europe

Technologies	Medium Term	Long Term
Industrial / Infrastructures monitoring for security (autonomous sensors) - on vibrating sources	Harvesting on industrial machines	
Develop wireless autonomous monitoring in transportation (car, planes…)	Harvesting on railway, train	Harvesting on cars, planes
Develop wearable systems for human movement harvesting	Shoes	Medical patches

Technology and design challenges

Power Amplifier Technology challenges	Medium Term	Long Term
Bio-compatibility	Piezo-electret, composites without lead	Nanotechnology, nanocomposites without lead
Low temperature integration, reduction of process temperature without affecting global performance	Composites, Piezo-electret	Nanotechnology, nanocomposites

Definition of FoMs or planned evolution

FoM / Planned Evolution	2023	2026	2029	2033
MEMS devices (f < 300 Hz, G < 0.5)				
FoM1: Volume power density (mW/cm^3)	1	1.15	1.3	1.5
FoM2: Surface power density (mW/cm^2)	0.15	0.165	0.18	0.2
Industrial devices: Piezoelectrics on flexible substrates (@50 Hz, 0.5 G)				
FoM3: Surface power density (mW/cm^2)	0.1	0.115	0.13	0.15

Other issues and challenges, interaction with other areas

- Interaction with “heterogeneous integration”
- Interaction with “Equipment and materials”

Concept 3: Mechanical EH: Electromagnetic transduction

The operating principle of electromagnetic energy harvesting devices is based on Faraday's law, which states that a relative motion between a magnetic field and an electrical coil or a change in the flux linkage with a coil induces an electromotive force (EMF) in that coil. The EMF depends on the strength of the magnetic field, the length of the coil, and the relative velocity (or flux linkage rate) between the magnetic field and the coil. The following equation represents this relationship:

$$EMF\ (V) = \frac{d\Phi}{dt} = Bl\frac{dx}{dt}$$

Where Φ is the total flux linkage; t is the time, and B, l, and x are the flux density, the effective length of the wire and the displacement between the magnets and the coil respectively. The relative motion between the magnetic field and the coil can be produced by moving the magnets with respect to the coil or vice versa. The coil can be either wire-wound or micro-fabricated. The electromagnetic energy harvesters which have been researched are either macro-sized structures or miniaturized structures utilizing micro electro mechanical system (MEMS) fabrication techniques. In general, the operational principle of electromagnetic induction based generators can be grouped into three types[3]: resonant, rotational, and hybrid devices. The main challenge in MEMS electromagnetic transducer research is the CMOS compatible integration of thick, high performance permanent magnets and development of low loss, multi-turn, micro-fabricated coils. Apart from that, wide bandwidth response, maintaining low operational frequency, improving the energy density and reliability are the key research challenges like any mechanical EH transduction mechanism.

Competitive situation for concept 3

Electromagnetic transduction is one of the most well researched and prominent method of transducing electricity from ambient mechanical vibrations. Among industries, EnOcean, Perpetuum (spin-off from Univ of Southampton, UK), Flexous (spin-off from TU Delft, Netherlands), Revibe (Germany) are active in this particular area. However, majority of the reported devices in literature and by industries are developed at macro to meso-scale level (~few cm^3 prototypes) using discretely assembled components. Such small scale devices show impressive performances with high level of reliability. Due to drastic drop of performanc-

3 A. Khaligh, P. Zeng, C. Zheng, Kinetic Energy Harvesting Using Piezoelectric and Electromagnetic Technologies—State of the Art, IEEE Trans. Indus. Elec., 57(3): 850-860 (2010).

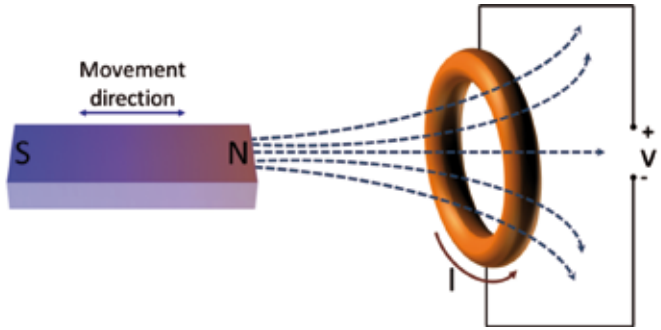

Fig. II.5.3: Illustration of Faraday's law that governs electromagnetic generators.

Key research questions/issues

Technologies	Medium Term	Long Term
Increasing the power density with miniaturization for most applications	Integration approaches of permanent magnets and coils	Developing high energy product integrated magnets; alternative hybrid transductions
Increasing the bandwidth of operation, while operating at low frequency ranges	Exploiting the nonlinearities, multiple nonlinearities in a single system, addressing the multi-stability issue	Frequency independent adaptable devices
Development of CMOS compatible, high performance micro/nano-magnets for MEMS/NEMS-scale integration	Thick, polymer bonded powdered permanent magnets; nano-structured, high energy product patterned magnet development	Thick, rare-earth free, nanocomposite, exchange coupled (soft/hard) magnet integration
Development of low loss, multi turn micro-coil fabrication method	Improving the packing density, aspect ratio, number of turns	MEMS compatible alternative methods for fabricating coils
Robust mechanical structure to sustain large amplitude vibrations – reliability	Polymer/flexible substrate; alternative spring structures; vacuum packaging to reduce mechanical losses	Alternative topologies incorporating nanowires/nanotubes

Application needs & Impact for Europe

Technologies	Medium Term	Long Term
Acoustic Emission Monitoring of industrial machines	Harvesting from, structural health monitoring of industrial machines	Monitoring of automated process manufacturing
Railroad monitoring. Automotive and aircraft sensor powering.	Harvesting on railway, train, car, aircrafts	Enabling smart sensing for automated transportation
Internet of Things – smart building management, smart environment	Harvesting on door movement; Smart devices – washing machine, refrigerator, computer, key board etc.	Enabling e-health, e-environment
Human wearable devices (f<10 Hz, 1-2 g)	Harvesting for body worn smart devices	In-vitro and in-vivo self-powered, micro-scale, biocompatible devices

Technology and design challenges

Power Amplifier Technology challenges	Medium Term	Long Term
Magnet-coil interaction – most important factor to improve the electromagnetic coupling per unit volume vis-à-vis the output voltage/power	Optimized patterned magnets to improve the EM coupling;	Suitable micro-coil topology with aligned magnet array to maximize the coupling
CMOS compatible permanent magnets for MEMS application	Looking beyond rare-earth free magnets: multi-nano-layers	Super hard, nano-structured integratable magnets

Definition of FoMs or planned evolution

FoM / Planned Evolution	2023	2026	2029	2033
Miniaturized devices (f < 100 Hz, G < 0.5)				
FoM1: Volume power density (mW/cm^3)	5	6.5	8	10
FoM2: Surface power density (mW/cm^2)	0.15	0.18	0.21	0.25
Fully integrated MEMS devices (f < 100 Hz, G < 1)				
FoM1: Volume power density (µW/cm^3)	10	37	64	100
FoM2: Surface power density (µW/cm^2)	2	7.4	12.8	20

es with scaling and complexity in fabrication steps, MEMS electromagnetic transducers are relatively less explored compared to other counterparts such as piezoelectric, electrostatic etc.

Recommendations for concept 3

- CMOS compatible integration technique for rare earth free, high energy product micro-magnets (with materials like CoPt, CoPtP and their nano-composites/hetero-structures).
- 3D coil integration/development having low resistive loss and enhanced turn numbers.
- Develop new concepts leading to performance and bandwidth improvement at low frequency (e.g. nonlinear dynamics, frequency-up converters, hybrid, adaptable devices).
- Device miniaturization and/or integration on flexible substrates would be a key to fit many applications such as self-powering human wearables.
- Packaging is also a key to improve performance and reliability, in particular vacuum packaging of individual devices in a batch fabrication process.
- Hybrid integration of multiple transducers (EM+piezoelectric, EM+triboelectric) to improve the device efficiency and power density.

Other issues and challenges, interaction with other areas

- Interaction with "heterogeneous integration"
  - Flipchip bonding of substrates containing micro-magnets and micro-coils to improve the electro-magnetic coupling/turn and vacuum packaging
- Interaction with "Equipment and materials"

Concept 4: Thermal energy harvesting

These devices convert thermal energy to electrical energy via the Seebeck effect[4]. There are two main technologies: bulk technology and thin film technology. The bulk technology is adapted for applications (e.g. automotive, industrial applications, etc.) for which the size of thermoelectric (TE) devices is not a constraint (size vary from some cm² to some tens of cm²) and for which high power is required (W to kW range). The thin film technology is adapted for the confined environment, for which the size is a key point (mm² to few cm²) and for which power from the µW to mW range is required. Most of the commercialized thin film TE devices are made of Bi_2Te_3 active materials (toxic/rare/expensive/not compatible with Si technologies). The main FoM is ZT, a dimensionless parameter defined by $ZT=\sigma S^2T/\lambda$, with σ the electrical conductivity, S the Seebeck coefficient, λ the thermal conductivity and T the temperature. For many years, Bi_2Te_3 has been the best TE material at room temperature with a ZT close to 1, and the objective would be to increase the ZT value up to 3.

4 Puscasu, O., Monfray, S., Savelli, G., Maitre, C., Pemeant, J. P., Coronel & Guyomar, D. (2012, December). An innovative heat harvesting technology (HEATec) for above-Seebeck performance. In Electron Devices Meeting (IEDM), 2012 IEEE International (pp. 12-5). IEEE.

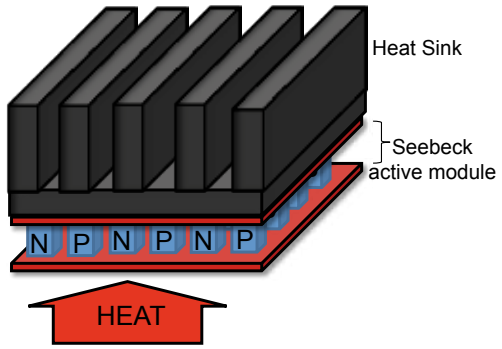

Fig. II.5.4: Basic Seebeck thermo-generatorstructure schematic with Heat sink

Competitive situation of Concept 4

All commercially available modules are based on Bi_2Te_3 material with a ZT value close to one (Laird Technology, Thermogen in USA and MicropeIt in Germany…). The main challenge in the future would be to reach similar and above performances with less rare material (like Si-based materials).

Recommendations for Concept 4

- From material point of view, new sustainable materials should be considered to avoid Bi_2Te_3 (i.e. Si based solutions, nanostructured materials…)
- Cost is a key point for energy harvesting: miniaturized solutions should focus on Si or SiGe material (nanostructured materials, phonon engineering) for compatibility with standard semi-conductor industries to reduce production costs.
- For non-miniaturized solutions, low cost and flexibles materials should be developed, with optimized thermal engineering at the product level to reduce the size of the heat sink.
- Improvement of ZT will allow heat sink size reduction
- New thermal energy approaches (non Seebeck) needs also to be developed (i.e. phase change of liquid, thermomechanical approaches, thermodynamic cycles…)

Other issues and challenges, interaction with other areas

- Power consumption of power management circuit in function of temperature.
- Increase reliability of integrated systems
- Develop low cost solutions / flexible materials
- Leakage of storage element at high temperature

Concept 4: Thermal energy harvesting

Key research questions/issues

Technologies	Medium Term	Long Term
Improve efficiency of thermal to electricity transformation near room temperature (<400 K)	ZT>2,5	ZT>3
Develop "green" solutions for near-room temperature use cases (<400 K), not based on Bi_2Te_3	Nanostructured materials / SiGe based solutions	Nanostructured materials / Si based solutions
Develop scalable technologies at low cost	SiGe based solutions (bulk & thin films)	Si based solutions (thin films)
Reduce the size of the "bulky systems" integrated with heat sink	Thermal engineering at product level	High ZT material

Application needs & Impact for Europe

Technologies	Medium Term	Long Term
Industrial monitoring for security (autonomous sensors)	Hvac, Hot pipelines, electrical installations	Hvac, Hot pipelines, pumps…
Infrastructure monitoring for security (autonomous sensors)	Pipe leaks, electrical lines	
Home automation for energy saving (autonomous sensors and heat systems monitoring)	Heating systems control, ETRV	Boiler tank, solar thermal monitoring
Develop wireless autonomous monitoring in transportation (car, planes…)	Sensors in cars (exhaust), trains	Sensors in cars (motor), planes

Technology and design challenges

Power Amplifier Technology challenges	Medium Term	Long Term
Develop new material for improved efficiency without Bi_2Te_3 near room temperature	Nano structured materials / SiGe based solutions	Phonon engineering / Si based solutions
Maintain the thermal gradient on thin devices / reduce size of heat sink: This can be addressed with ZT improvement, system architecture and heat sink engineering	ZT>2,5	ZT>3
Develop alternatives to Seebeck approaches	Phase change solutions (materials, liquids) or thermomechanics approaches	Alternative solutions at microscale

Definition of FoMs or planned evolution

FoM / Planned Evolution	2023	2026	2029	2033
ZT	>2.5	2.65	2.8	>3
Expected Output power vs available temperature difference on the TEG ($mW/K^2/cm^2$) in function of area (based on Tcold=300K)	>0.15 $mW/K^2/cm^2$	0.165	0.18	>0.2 $mW/K^2/cm^2$

Concept 5: Photovoltaic Energy Harvesting

Photovoltaic (PV) effect consists in the absorption of light by the semiconductor, generation of electron-hole pairs and collection of charge carriers (thanks to the semiconductor device), allowing the generation of power (see Fig. II.5.5[5]).The FoM usually used for solar cells working under sun light is the power conversion efficiency (output power density divided by incident sun power density of 1 kW/m^2, Solar spectra: AM1.5@ 25 °C). However, the output power density of the solar cell is depending on the incident light intensity, absorption and electronic properties of the material, spectral sensitivity of the solar cell to the light, electronic quality and properties of the semiconductor device. Therefore for solar cells working in indoor conditions, standard outdoor measurement conditions are not relevant because artificial modern light (fluorescent, LED) present a different spectrum and far lower intensity compared to sunlight. For indoor light conditions, the parameter usually used is the output power density under specified artificial light intensity, but no standard measurement conditions are defined. But the Schokley limit efficiency of an ideal photovoltaic cell for various indoor radiation sources is higher than in outdoor condition. For example with a fluorescent tube and a bandgap Eg =1.95 eV the limit is 67%.[6] For a white LED and a bandgap Eg =1.9 eV the limit is 57%[7] The photovoltaic production is dominated by silicon based solar cells due to its abundance, well-known and mature technology thanks to microelectronic industry. Indeed most of the outdoor commercialized solar cells are made of crystalline silicon (c-Si) and for indoor applications amorphous Si (a-Si) solar cells are commercialized. For outdoor solar cells, thin film cells (CdTe, CIGS, a-Si, organic, dye) are also commercialized, as well as high efficiency solar cells working under concentrated sun light[8 9 10 11]. Similarly, for indoor applications, photovoltaic cells are also commercialized based on materials other than Si like for example III-V compounds, dye, organic…

5 http://panasonic.co.jp/es/pesam/en/products/pdf/Catalog_Amorton_ENG.pdf

6 Mo. Freunek, Mi. Freunek, and L. M. Reindl, Maximum Efficencies of Indoor Photovoltaic Devices, IEEE JOURNAL OF PHOTOVOLTAICS, VOL. 3, NO. 1, JANUARY 2013

7 Nathalie Carrier, Indoor photovoltaics with Perovskite solar cells and nanostructured surfaces. TRITA-FYS, 2016:01. Master thesis KTH, Applied Physics. http://www.diva-portal.org/smash/record.jsf?pid=diva2%3A898443&dswid=9979

Competitive situation for concept 5

If light is available for a given autonomous application, the photovoltaic principle is the best choice among all the harvesting technologies (especially in outdoor conditions) providing the highest electrical power density. Silicon technology is very mature for these outdoor conditions (Jinko Solar, Canadian Solar, Hanwha Q-cells, Sunpower…) but also for indoor (Panasonic in Japan, Solems in France…). However, other firms are commercializing, for indoor and/or outdoor energy harvesting applications, high efficiency, transparent and/or flexible solar cells (AltaDevices, G24 Power in UK, Sunpartner in France, OPVIUS in Germany…) made of different materials (III-V compound, dye, organic…) than Si.

8 Technology Roadmap, Solar Photovoltaic Energy, IEA, 2014

9 International Technology Roadmap for Photovoltaic (ITRPV) 2017

10 Photovoltaic Report, Fraunhofer ISE, 2018

11 Current Status of concentrator photovoltaic (CPV) technology, Fraunhofer ISE, NREL, 2016

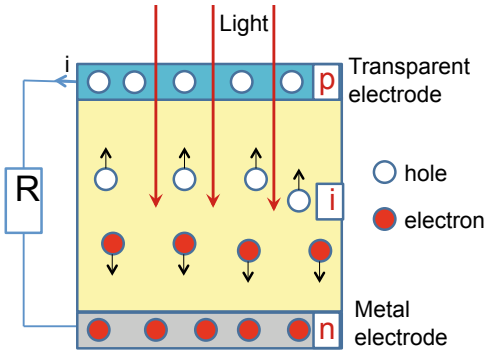

Fig. II.5.5: a-Si pin solar cell

Concept 5: Photovoltaic Energy Harvesting

Recommendations for concept 5

- Define standard procedures for indoor photovoltaic cells characterization (light intensity and spectra, direct and diffuse light, temperature…) and for transparent photovoltaics (see footnote 7, on p. 71).
- Design and optimize structures for outdoor or/and indoor light and for different type of applications: sensitivity to different light sources (sun, artificial light, diffuse and/or direct light), flexibility and/or transparency if necessary, cost, output power, material abundance (especially for mass production such as outdoor applications).
- a-Si is the most used material for indoor energy harvesting and c-Si for outdoor photovoltaic. However other materials and structures (dye, III-V compounds, organic…) present interesting potential for indoor energy harvesting providing flexibility, transparent PV, high output power, etc. For some of those materials it is recommended to decrease the cost (III-V compounds, multijunction, nanostructured) and increase lifetime and/or stability (perovskite,organic).

Other issues and challenges, interaction with other areas

- Interaction with “heterogeneous integration”
- Interaction with “Equipment and materials”
- Decrease the consumption of associated management circuits

Key research questions/issues

Technologies	Medium Term	Long Term
Improve PV (photovoltaic) cell output power density for indoor applications	Organic, DSSC (Dye Sensitized Solar Cells), semiconductors compounds (III-V, CdTe,…), a-Si, Perovskite	Perovskite, Multi-junction PV cell, nanostructured materials…
Improve PV cell output power density for outdoor applications	Si solar cells, tandem cells on Si, semiconductors compounds (CdTe, CIGS…), DSSC, Organic	Multi-junctions, nanostructured materials, quantum dots…
Develop flexible, stable, high power conversion efficiency and low cost PV cells. Develop high efficiency and low cost transparent photovoltaic[1]	Thin-film PV cells (III-V, organic, DSSC…)	Thin-Film (perovskite…), multi-junctions, nanostructured…

Application needs & Impact for Europe

Technologies	Medium Term	Long Term
(Bottom-up) Autonomous systems : portable devices, IoT, health applications	Sensors, IoT, portable electronic devices, home automation, security systems, automotive…	IoT, health applications, factory automation, smart buildings…

Technology and design challenges

Power Amplifier Technology challenges	Medium Term	Long Term
Optimize the structure of the solar cell for Indoor and/or outdoor applications.		
Increase the efficiency and reduce the cost of PV cells for energy harvesting applications. When needed (perovskite…), improve stability and lifetime of the solar cell.	Commercialized organic and inorganic (III-V compounds, DSSC…) for indoor and outdoor applications with improved efficiency and low cost	Low cost PV cells with increased efficiency (III-V compounds, multijunction, nanostructured, thin film, perovskite…)

1 C.J. Traverse et al, Emergency of highly transparent photovoltaics for distributed applications, Nature Energy, vol. 2 849-860 (2017)

Definition of FoMs or planned evolution

FoM / Planned Evolution	2023	2026	2029	2033
Commercialized output power density (W/cm^2) and efficiency under standard output sunlight conditions (AM1.5G, 1 kW/m^2, 25 °C)	• >23 mW/cm^2 (efficiency : 23%) for c-Si cells • >18% CdTe or CIGS cells • >13% a-Si, organic, DSSC	• >23.6 mW/cm^2 (efficiency : 23.6%) for c-Si cells • >19.2% CdTe or CIGS cells • >13.9% a-Si, organic, DSSC	• >24.2 mW/cm^2 (efficiency : 24.2%) for c-Si cells • >20.4% CdTe or CIGS cells • >14.8% a-Si, organic, DSSC	• >25 mW/cm^2 (efficiency : 25%) for c-Si cells • >22% CdTe or CIGS cells • >16% a-Si, organic, DSSC
Commercialized output power density (W/cm^2) for indoor modern artificial light conditions (200 lux, LED or fluorescent)	>20 µW/cm^2	>21.5 µW/cm^2	>23 µW/cm^2	>25 µW/cm^2

Concept 6: RF energy harvesting/wireless power transfer

The wireless delivery of RF power has been used for many years and for various applications and power needs: from relatively large unmanned systems and associated power needs to very small battery-less devices[12].

To reach this goal, two physically different mechanisms can be used: i) the so-called Far-Field Wireless Power Transfer (FF-WPT), which exploits the radiated far-field radio-frequency (RF) sources, either in the microwave (300 MHz -30 GHz) or millimeter-wave (30 GHz – 300 GHz); ii) the Near-Field Wireless Power Transfer (NF-WPT), which exploits the near- (or reactive-) EM field in the low-frequency (LF: 30-300 kHz) or high-frequency (HF: 3-30 MHz). In the FF-WPT case the radiation of an electromagnetic (EM) wave occurs through the exploitation of a radiating structure (antenna), and the corresponding radiated RF power can be intentional (in the case of FF-WPT) or unintentional/environmental (in the case of RF Energy Harvesting (EH) application).

When far-field sources are involved, no direct interactions between the transmitting (TX) and receiving (RX) antenna take place, because the TX antenna sends the same amount of power weather or not a receiver is present. In the non-radiative NF-WPT case, inductive links (exploiting magnetic field) or capacitive links (exploiting electric fields) are established between co-located coils/wires or electrodes/metallic plates, respectively: being in the reactive field region, the power delivered by the TX coil/plate may be strongly affected by the presence and location of the RX coil/plate, if suitable design choices are not followed. As regards the commercial/research applications, the FF approach is mainly deployed when low- (FF-WPT) or ultra-low (EH) power applications are envisaged. Only in space and military targets, where the costs are not an issue, high-power FF-WPT activities are present. For these reasons the two approaches are almost complementary, as summarized on the right.

Despite of the completely distinct physical mechanisms of the NF and FF WPT, the wireless link building blocks can be depicted in a unified vision as in the Figure below: planar coils and planar microstrip antennas are used as representative of the two transmission mechanisms, but capacitive-coupled links or other antenna types can be adopted equivalently. A unified Figure-of-Merit (FoM)[13], representing the end-to-end efficiency of the whole system, from the transmitter DC bias to the receiver dc output, can be expressed in both cases as:

$$\eta_{LINK} = \eta_{DC-TF} \cdot \eta_{TF-TF} \cdot \eta_{TF-DC} = \frac{P_{TX}}{P_{BIAS}} \cdot \frac{P_{RX}}{P_{TX}} \cdot \frac{P_{DC}}{P_{RX}}$$

The first term, ηDC-TF, is the ratio between the power P_{TX} available at the transmitting antenna/coil input port and the DC power consumed by the transmitter, P_{BIAS}. The second term, ηTF-TF, is the link efficiency of the wireless path: it consists of the ratio between the power received by the antenna/coil at the receiver side (P_{RX}) and P_{TX}; it is strongly dependent on the medium in between the transmitter and the receiver, and on the antennas/coils efficiencies. Finally, the last term, ηTF-DC, is the ratio between the DC power delivered to the final user (P_{DC}) and the received one (P_{RX}), i.e. the conversion efficiency of the rectifying section from the higher frequency to DC.

	NF-WPT		FF-WPT
	Resonant	Non-resonant	
TX mechanism	Coupling, no wave propagation	Coupling, no wave propagation	Wave propagation
Interacting device	Coils/electrodes	Coils/electrodes	Antennas
TX-RX interaction	Strong interaction	Medium interaction	No interaction
Operating frequency	LF, HF	LF, HF	microwave, millimeter-wave
Distance	mm to few cm	Tens of cm	cm to tens of meters
Transferred RF Power	Medium (W), high (kW)	Medium (mW-W)	Ultra-low (few μW), low (hundreds of μW, few mW),
Efficiency	High (70-90%)	Medium (30-60%)	Low (10-50%)
Commercial applications	Yes	Yes	No

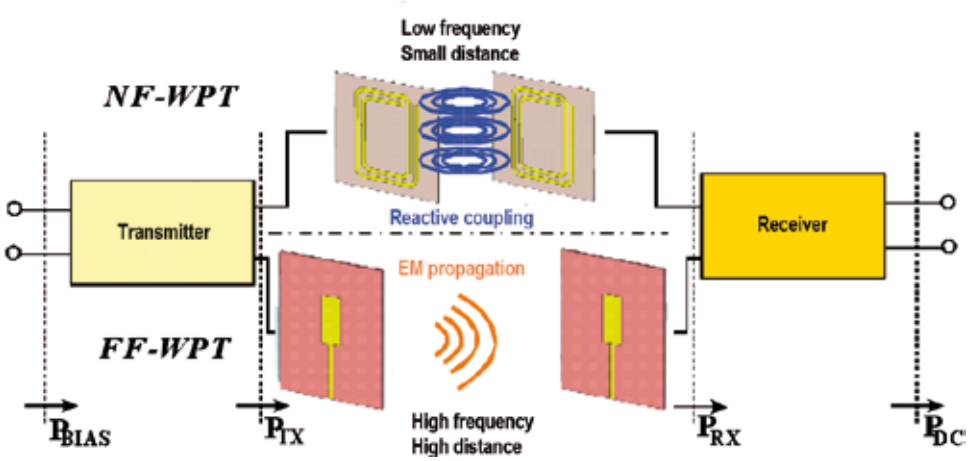

Fig. II.5.6: End-to-end block representation of a wireless link involving either near- or far-fields[14].

12 N.Borges Carvalho et al., "Wireless Power Transmission: R&D Activities Within Europe," in IEEE Transactions on Microwave Theory and Techniques, vol. 62, no. 4, pp. 1031-1045, April 2014. doi: 10.1109/TMTT.2014.2303420

13 Costanzo, A., Dionigi, M., Masotti, D., Mongiardo, M., Monti, G., Tarricone, L., Sorrentino, R. "Electromagnetic energy harvesting and wireless power transmission: A unified approach", (2014) Proceedings of the IEEE, 102 (11), art. no. 6916985, pp. 1692-1711. DOI: 10.1109/JPROC.2014.2355261.

14 M. Piñuela, P. D. Mitcheson and S. Lucyszyn, "Ambient RF Energy Harvesting in Urban and Semi-Urban Environments," in IEEE Transactions on Microwave Theory and Techniques, vol. 61, no. 7, pp. 2715-2726, July 2013. doi: 10.1109/TMTT.2013.2262687

Concept 6: RF energy harvesting/wireless power transfer

Competitive situation of concept 6

Remote RF energy reception is foreseen as a robust solution for powering battery-less devices pervasively distributed in the environment of several application domains such as: environmental monitoring, industrial plants and e-health. Given the presence of RF sources in most humanized environments, harvesting the ambient available RF energy has been widely investigated and experimented but it can be concluded that, due to the measured ultra-low power densities[15] and its uncertainties, it cannot guarantee the needed energy even for powering devices with uW needs. Indeed a minimum power is needed to turn on the rectifying circuits, which, for the currently available devices, should be higher than 10 uW. On the contrary, providing RF power "on demand" by means of distributed dedicated sources equipped with "smart" beaming techniques is a promising option guarantying at the same time proper rectifier activation and minimum wasted RF energy.

Furthermore the RF signal shape optimization is foreseen to cope with these constrained by dynamically duty-cycling the power signal in order to provide higher power peaks, in selected time slots while maintaining the same average power over the period[16].

Recommendations for concept 6

Define the minimum RF power needed to activate the rectifier circuit and optimize/minimize the rectenna components to minimize losses and to maximize the power transfer.

Optimize the conversion efficiency over the range of expected RF powers and the expected load as the best compromise between converted DC power and minimum DC voltage, that is over the optimum DC loads. This means that the nonlinear behavior of the RF circuits need be accounted for in a unique design procedure and that a co-design of the PMU is highly appropriate.

Design high efficient receiving antennas with miniaturization constraints in order to maximize the received power. To cooperate with this goal the mm-wave range will be investigated in the next future and is foreseen as a promising solution for distances under one meter.

15 M. Piñuela, P. D. Mitcheson and S. Lucyszyn, "Ambient RF Energy Harvesting in Urban and Semi-Urban Environments," in IEEE Transactions on Microwave Theory and Techniques, vol. 61, no. 7, pp. 2715-2726, July 2013. doi: 10.1109/TMTT.2013.2262687

16 Del Prete, M., Costanzo, A., Magno, M., Masotti, D., Benini, L, "Optimum excitations for a dual-band microwatt wake-up radio", (2016) IEEE Transactions on Microwave Theory and Techniques, 64 (12), art. no. 7747520, pp. 4731-4739. DOI: 10.1109/TMTT.2016.2622699.

Key research questions/issues

Technologies	Medium Term	Long Term
a) Transmitter side: Combining beam-forming and signal design to provide directive power transmission. b) Receiver side: compact antenna solution	Exploitation of the signal theory to enhance the link efficiency at ultra-low RF received power levels (under 1 uW)	mm-wave reconfigurable RF sources and miniaturized power receivers
Devices for rectifying the RF sources main requirements: high dynamic range, compact receiving antenna solutions.	New rectifier topologies based on CMOS technologies rather than on discrete components	Miniature systems integrating the antenna and the rectifier circuit in CMOS technology with RF-to-DC efficiency comparable with Shottcky-diode based topologies
Characterization of non- conventional materials for the rectenna design	Wearable solutions for e-health monitoring based on flexible antenna	Implanted miniaturized rectennas

Application needs & Impact for Europe

Technologies	Medium Term	Long Term
Wearable electronics	Body sensors for sport or for worksuits…	Smart clothes/textiles…
Implantable electronics / biomedical devices	Basic wearable monitoring of physiological parameters (temperature, ECG, motion, etc.) leadless pace-maker	Implantable chips for monitoring physiological/biochemical parameters, or for being embedded in smart prosthesis
Environmental monitoring	Miniature energy autonomous nodes powered by multiple sources	More efficient implementations
Industrial applications (smart machinery parts)	Smart machinery parts (e.g. rotating)	More efficient implementations
Automotive	On-board and on-engine wireless sensor networks	More efficient implementations
Logistics and tracking goods	Smarter UHF RFID tags with enhanced functions, such as localization, sensing, datalogging, on multiple chips and components.	Single-chip cost-effective RFID-like tags

Technology and design challenges

Power Amplifier Technology challenges	Medium Term	Long Term
Integrated design of the antenna and rectifier for large dynamic range	Development of auto-adjusting solutions by sensing the received RF power and exploiting the self-bias mechanism of ultra-low power transistor.	High dynamic range rectennas
Design of dedicated signals for enhancing the power transfer	Proof-of-concept demonstrators of dynamically varying power transmission	Power shaping sources adjustable in real-time

Definition of FoMs or planned evolution

FoM / Planned Evolution	2023	2026	2029	2033
Miniaturized Antenna radiation efficiency	> 50 %	> 56 %	> 62 %	> 70 %
Increase RF-to-DC conversion efficiency at low-power levels (1µW)	> 20%	> 26%	> 32%	> 40%

Concept 7: Energy storage - Microbatteries

Microbatteries for energy storage processed on Si have to date achieved volumetric energy densities approaching 1 mWh/cm^2 with µm scale lithium-based thin film materials, offering capacity retention over thousands of cycles[17]. In the 2D, thin-film geometry, current deposition techniques and lithium ion diffusion limits the electrode thickness to several micrometers resulting in a battery dominated by the substrate and other inactive cell components. Silicon integrated microbatteries are also typically solid-state utilizing vacuum deposited thin film electrodes and solid electrolytes. The ionic conductivity of the all solid-state electrolytes are usually orders of magnitude lower than the more common liquid based electrolytes of commercial lithium ion batteries. There are ongoing efforts to develop new electrolytes with higher conductivity. Alternative battery couples such as those based on multivalent aluminium or magnesium may also lead to improvements in the energy density per unit volume and significant cost savings through the use of more abundant materials although significant research is required to develop rechargeable versions competitive with the long-life lithium based options. In the near term developments with lithium based chemistries that can improve the capacity per unit footprint include multilayer deposition which requires development of appropriate patterning techniques as the typical vacuum systems result in blanket deposits. Other options include 3D substrate structuring and thicker electrode processing to increase the storage density while maintaining the power capability[18] [19]. 3D printing of active materials on low cost substrates is of interest to high aspect ratio structures with enhanced capacity per substrate area even allowing for the decreased density of the materials and use of pastes.

17 Dudney, N. J. Mat Sci. Eng B-Solid 2005, 116, 245.

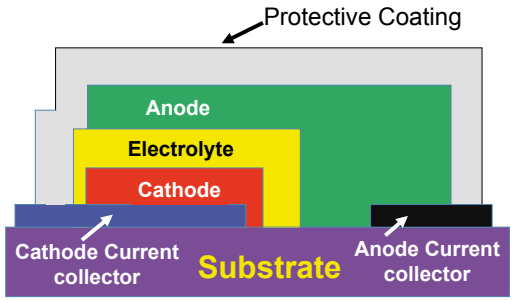

Fig. II.5.7: Typical thin film microbattery structure (overall thickness ~10 µm)

Competitive situation of concept 7

By comparison with capacitors, supercapacitors or commercial Li-ion batteries, microbatteries offer several advantages: Like most batteries they offer higher energy density than capacitors and significantly lower leakage currents (nA). They also offer improved safety over conventional batteries (no toxic liquid; biocompatible), thermal stability up to 150°C and expected long life (10 years). With microfabrication, small size is possible to the mm-scale and possibly smaller if required for niche applications. Another advantage is to enable the energy storage device to be closer to the load and have an integrated module.

Thin film integrated microbatteries are the option being investigated for distributed sensors coupled with energy harvesting and micropower management. Europe has globally competitive expertise in storage technologies (i.e. Ilika Technologies in UK and STMicroelectronics in France/Italy), energy harvesting and management options.

18 W. Wang, J.F. Rohan, N. Wang, M. Hayes, A. Romani, E. Macrelli, M. Dini, M. Filippi, M. Tartagni and D. Flandre, Chapter 9 - Smart Energy Management and Conversion in Beyond CMOS Nanodevices 1 (2014) Editor F. Balestra, Wiley, P 249-276, ISBN: 978-1-84821-654-9

19 J.F. Rohan, M. Hasan, S. Patil, D. Casey and T. Clancy, Chapter 6 – Energy storage materials and architectures at the nanoscale, in ICT-Energy - Nanoscale energy management concepts towards Zero-Power Information and Communication Technology / (2014) Editors, G. Fagas, L. Gammaitoni, D. Paul and G. Abadal Berini, Intech Publications, Croatia. pp 107-138, ISBN 980-953-307-1005-8, DOI: 10.5772/57139

Key research questions/issues

Technologies	Medium Term	Long Term
Improve capacity with a reduced surface area and volume	Multilayer microbattery structure Thick film materials deposition.	New lithium based electrode and electrolyte materials. Multivalent electrode systems
Increase power capability for portable applications, adaptable devices	3D structuring	With new materials
Increase performance of electrode and electrolyte materials	Higher conductivity materials	Interface engineering for optimised performance
Processing on low cost substrates	3D printing	High density materials Non volatile electrolytes

Application needs & Impact for Europe

Technologies	Medium Term	Long Term
Internal autonomous sensors	Factory	Home
External autonomous sensors	Environment	Agriculture
Develop healthcare systems	Medical patches	Implantable

Technology and design challenges

Power Amplifier Technology challenges	Medium Term	Long Term
Patterning active materials	Decrease waste	Increase loading for higher capacity
Low temperature integration, reduction of process temperature without affecting global performance	On silicon	On flexible substrates
Packaging of microbattery device	Reliable	Low cost

Definition of FoMs or planned evolution

FoM / Planned Evolution	2023	2026	2029	2033
FoM1: Surface energy density (mWh/cm^2)	5	6.5	8	10
FoM2: Surface power density (mW/cm^2)	10	13	16	20
FoM3: Cycle life	10,000	13,000	16,000	20,000

Recommendations for concept 7

- Multilayer materials processing for increased capacity per unit footprint.
- Patterning of active materials to decrease waste and increase architecture development.
- New materials to increase ionic conductivity for electrolytes and electronic conductivity for both electrodes.
- Higher energy density materials to decrease footprint requirements
- Packaging and integration with energy harvesting and micro power management modules.

Concept 8: Energy storage - Microcapacitors

Microcapacitors integrated on Si with monolithic integrated circuits (ICs) have been typically dedicated to RF, timing, filtering, or A/D conversion applications, which require small to moderate capacitance[20] [21]. More recently, great efforts have been dedicated to integrate the full power supply and thus microcapacitors on-die[22], in combination with a variety of Si-based energy harvesting devices, sensors and transmission circuitry, leading towards truly autonomous sensor systems.
The main advantages of microcapacitors compared to other alternatives for micro-energy storage applications, namely microbatteries, electrolytic capacitors and supercapacitors, are their robustness of operation and ease of integration, stemming from the lack of need for an electrolyte. Another important advantage is the much higher voltage of operation than the mentioned alternatives due to much lower leakage currents. Furthermore, microcapacitors use materials which are environmentally and health friendly. Their main drawback so far is their limited value of capacitance density and, therefore, energy storage capability[23].

Three main parameters need to be optimized in microcapacitors for energy storage moving forward: the capacitance density, the leakage current and the series resistance. The first affects the maximum energy which can be stored, the second affects the maximum voltage of operation, the maximum stored energy and the retention characteristics of the device, while the third affects the charging and discharging times and hence the power which can be generated, as well as the maximum operating frequency. The capacitance density should be maximized, while the leakage current and series resistance should be minimized.

There are two main strategies to increase the capacitance density of a microcapacitor: a) increase the capacitor surface area or b) optimize the materials used and mainly the dielectric material parameters (reduce the thickness or increase the dielectric constant). The dielectric constant and layer thickness constitute very important factors towards increasing the capacitance density. High-k materials are the ferroelectric and paraelectric materials. However, ferroelectric materials with very large dielectric constants (> 1000) should be excluded due to a variable dielectric constant which depends on the applied voltage, temperature and operating frequency. They also show severe aging effects. The remaining choice is the use of paraelectric materials with moderate dielectric constant, which are currently adopted. The option of reducing the dielectric layer thickness in order to increase the capacitance density is also used. However, the significant reduction of the dielectric layer thickness induces an increase of the leakage current. Thus, by using very thin high-k dielectrics very high values of capacitance density have been achieved so far both in MIM and MIS capacitor architectures, albeit without the optimization of the other two critical microcapacitor parameters, the leakage current and the series resistance. The absence of simultaneous optimization of all parameters involved in energy storage is the main challenge moving forward. The other challenging strategy is to increase the capacitor surface area through 3D structuring of the electrode surface. Advanced nanotechnology processes are needed in this respect. Increasing the capacitor surface area has been typically achieved by etching or sintering, or by using nanoporous materials with vertical pores or vertically aligned Si nanowires (SiNWs). Nanoporous alumina, porous Si, or Si nanowires by metal-assisted chemical etching (MACE) have been used as templates. Large capacitance densities have been reported using 3D structuring. Capacitance densities up to 100 μF/cm^2 were reported in [24], although these capacitors had very low operating frequency (<100 Hz), high leakage current and low breakdown voltage. Typical values of capacitance density obtained in the literature with moderate leakage current and breakdown voltage are of the order of 5-10μF/cm^2, Rs ~ 1Ω and operation frequency up to few kHz[25].

In the short term the use of optimized dielectric layers and electrodes, as well as optimized device geometries have to be addressed in order for the leakage current and series resistance parameters to be minimized without significant loss of the capacitance density. In the longer term more aggressive 3D structuring in combination with optimized high-k materials and geometries should be used for increasing the capacitance density, however without compromising the other two key parameters of the capacitor, namely the low leakage current and low series resistance.

Competitive situation of concept 8

Compared to other micro-devices for energy storage, namely micro-batteries, electrolytic capacitors and supercapacitors, microcapacitors offer significant advantages. The lack of an electrolyte makes these devices more robust in operation and also allows for much easier integration with batch Si technology. In addition, the materials used for their fabrication are environmentally and health friendly, safe and abundant.

Recommendations for concept 8

- Uniform thin high-k dielectrics showing reduced leakage currents and uniform coverage of the capacitor area
- High aspect ratio dense 3D structures for high capacitance density, combined with high-k uniform thin dielectrics (single layers or stack of them), optimized for increased energy per unit footprint, increased retention and operating frequencies
- Combination of the above with thicker metallic electrodes and new electrode materials for decreased series resistance
- Packaging and integration with energy harvesting and micro power management devices.

20 R. Ulrich and L. Schaper, "Materials options for dielectrics in integrated capacitors," in Proc. Int. Symp. Adv. Packag. Mater., Process., Properties Inter., 2000, pp. 38–43

21 E. Hourdakis and A. G. Nassiopoulou "Reaching state-of-the art requirements for MIM capacitors with a single-layer anodic Al2O3 dielectric and imprinted electrodes, Appl. Phys. Lett. 111, 033503 (2017); doi: 10.1063/1.4993898

22 M. Brunet and P. Kleimann, "High-density 3-D capacitors for power systems on-chip: Evaluation of a technology based on silicon submicrometer pore arrays formed by electrochemical etching," IEEE Trans. Power Electron., vol. 28, no. 9, pp. 4440–4448, 2013

23 M. Burke, A. Blake, V. Djara, D. O'Connell, I. M. Povey, K. Cherkaoui, S. Monaghan, J. Scully, R. Murphy, P. K. Hurley, M. E. Pemble, and A. J. Quinn, "High aspect ratio iridescent three-dimensional metal–insulator–metal capacitors using atomic layer deposition," J. Vac. Sci. Technol. A Vacuum, Surfaces, Film., vol. 33, no. 1, p. 01A103, 2015.

24 M. Burke, A. Blake, V. Djara, D. O'Connell, I. M. Povey, K. Cherkaoui, S. Monaghan, J. Scully, R. Murphy, P. K. Hurley, M. E. Pemble, and A. J. Quinn, "High aspect ratio iridescent three-dimensional metal–insulator–metal capacitors using atomic layer deposition," J. Vac. Sci. Technol. A Vacuum, Surfaces, Film., vol. 33, no. 1, p. 01A103, 2015.

25 Didac Vega, Jordi Reina, Ramón Pavón, and Angel Rodríguez, High-Density Capacitor Devices Based on Macroporous Silicon and Metal electroplating, IEEE Transactions on electron devices, Vol. 61, No. 1, january 2014

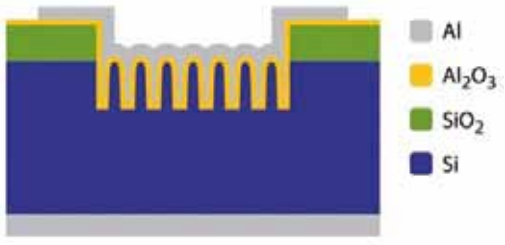

Fig. II.5.8: Schematic diagram of a Si-nanowire-based MIS capacitor.

Concept 8: Energy storage - Microcapacitors

Key research questions/issues

Technologies	Medium Term	Long Term
Improve capacitance density	3D structuring and use of known high-k materials(single layers or stack of them)	3D structuring in combination with new materials and device geometries
Reduction of leakage current	Use of optimized dielectric layers and other device materials	New materials
Reduction of series resistance	Thicker electrodes	Higher conductivity materials

Application needs & Impact for Europe

Technologies	Medium Term	Long Term
Internal autonomous sensors	Factory	Home
External autonomous sensors	Environment	Agriculture
Develop healthcare systems	Medical patches	Implantable

Technology and design challenges

Power Amplifier Technology challenges	Medium Term	Long Term
3D structuring of the capacitor surface area	Capacitance density 5- fold of that of the flat capacitor	Capacitance density 10-fold of that of the flat capacitor
Uniform high-k deposition	Known high-k materials	New materials not yet used in this application
Integration with on-chip harvesters	Design	Implementation

Definition of FoMs or planned evolution

FoM / Planned Evolution	2023	2026	2029	2033
FoM1: Capacitance density ($\mu F/cm^2$) combined with reduced leakage current (<1nA/cm^2) reduced series resistance (ESR ~ 1Ω) V_{max} = 5 V frequency of operation ~ 1MHz	10	22	34	50
FoM2: Series resistance (Ω)	1	0.73	0.46	0.1
FoM3: V_{max} (V)	5	6.5	8	10

Concept 9: Micro-Power Management (PM)

In order to take advantage from energy transducers, it is essential to develop electronic circuits for converting power, storing energy, and distributing it to application circuits efficiently, consuming less than the available input power. The design must tackle several trade-offs in achieving: (i) the PM circuits bias the source in its maximum power point (MPP); (ii) High efficiency in power conversion; (iii) the lowest intrinsic power consumption.

The most important FoM, which determine the low operating boundaries, are the intrinsic power consumption and the minimum input voltage, either during steady-state operation or during a cold start-up. Other FoMs include efficiency, and the surface area of the whole converter circuit. Commercial discrete components allow cost-effective solutions with intrinsic consumptions down to 1 µA and input voltages down to few tens of mV[26],[27]. CMOS implementations go further and achieve from hundreds nW[28] down to few nW[29].

26 S. Boisseau, P. Gasnier, M. Gallardo, G. Despesse, Self-starting power management circuits for piezoelectric and electret-based electrostatic mechanical energy harvesters, in: J. Phys. Conf. Ser., IOP Publishing, 2013: p. 012080. doi:10.1088/1742-6596/476/1/012080.

27 A. Camarda, A. Romani, E. Macrelli, and M. Tartagni, "A 32 mV/69 mV input voltage booster based on a piezoelectric transformer for energy harvesting applications," Sensors Actuators A Phys., vol. 232, pp. 341–352, May 2015.

28 M. Dini, A. Romani, M. Filippi, and M. Tartagni, "A Nano-Current Power Management IC for Low Voltage Energy Harvesting," IEEE Trans. Power Electron., vol. 31, no. 6, pp. 4292–4304, 2015.

29 W. Jung, S. Oh, S. Bang, Y. Lee, D. Sylvester, and D. Blaauw, "A 3nW fully integrated energy harvester based on self-oscillating switched-capacitor DC-DC converter," in 2014 IEEE International Solid-State Circuits Conference Digest of Technical Papers (ISSCC), 2014, pp. 398–399.

Competitive situation of concept 9

Power management circuits are essential to autonomous systems, and CMOS implementations have demonstrated dramatic reduction of the accepted input power and voltages. Major silicon foundries have proposed in the last years dedicated products operating down to few µW and few hundreds mV, along with very tiny implementations requiring few components. (STMicroelectronics in Europe, Texas Instruments, Analog Devices, Linear Technology, etc.)

Recommendations for concept 9

- Refinement of energy-aware nano-power design techniques for micro-power management circuits, in order to define adequate trade-offs between intrinsic power consumption, efficiency and performance.
- Power-constrained re-design of WSN circuits is recommended. This is key for application compatibility and to further reduction in intrinsic power of converters

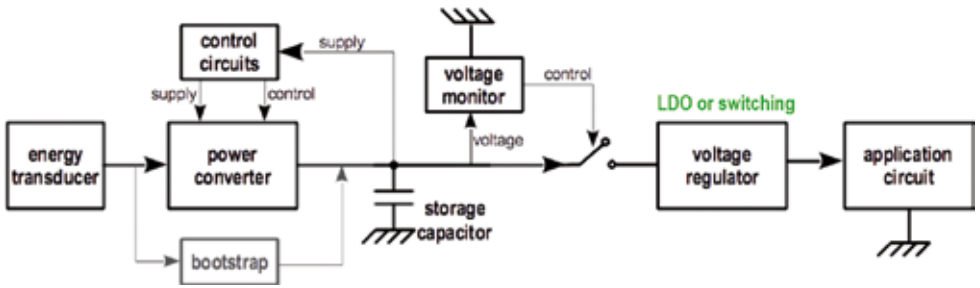

Fig. II.5.9: Block diagram of a battery-less power conversion and management system including a duty-cycled load. Ref: A. Romani et al., IEEE Computer 2017

Concept 9: Micro-Power Management (PM)

Key research questions/issues

Technologies	Medium Term	Long Term
Achieve operation with ultra-low input voltage and power levels (minimization of self-consumption and trade-offs with efficiency)	Power conversion/management ICs operating with < 1 µW and starting with 50-100 mV	Integrated SoC or SiP embedding power conversion/management and their specific functions operating in the 10-100 nW range
Perform battery-less start-up from fully discharged state	Fully integrated step-up converters based on low-VTH/native MOSFETs down to 50 mV. Integrated step-up converters aided by external magnetic or piezoelectric transformers down to few mV	Miniature systems with embedded micro-transformers (magnetic or piezoelectric) at package level starting from few mV
Are external passive required (C, L) or can the circuit be fully integrated? Overall size.	More efficient fully integrated inductor-less switched-capacitor converters Miniaturization of magnetic components	Development of alternatives of inductors for power conversion compatible with wafer-level processing, such as MEMS piezoelectric transformers Nanopower SoC and miniature passive + energy transducer integrated at package level (mm-scale systems)
Type of maximum power point tracking and/or source impedance matching provided	FOCV or derived techniques for DC sources with more responsive MPPT. Cancellation of reactive components of source impedance in vibrational energy harvesters	More complex MPPT algorithms implemented on-chip with ultra-low consumption
Reduce the power consumption of power management circuit	<1 µW / 70% efficiency	<100 nW / 80% efficiency

Application needs & Impact for Europe

Technologies	Medium Term	Long Term
Wearable electronics	Body sensors for sport or for worksuits	Smart clothes/textiles
Implantable electronics / biomedical devices	Basic wearable monitoring of physiological parameters (temperature, ECG, motion, etc.)	Implantable chips for monitoring physiological/biochemical parameters, or for being embedded in smart prosthesis
Environmental monitoring	Miniature energy autonomous nodes powered by multiple sources	More efficient implementations
Industrial applications (smart machinery parts)	Smart machinery parts (e.g. rotating)	More efficient implementations
Automotive	On-board and on-engine wireless sensor networks	More efficient implementations
Logistics and tracking goods	Smarter UHF RFID tags with enhanced functions, such as localization, sensing, datalogging, on multiple chips and components.	Single-chip cost-effective RFID-like tags

Technology and design challenges

Power Amplifier Technology challenges	Medium Term	Long Term
Power management distributed at many levels	Development of energy-aware circuit design techniques for power converters in the 1-100 nA range	Energy-aware design of all system parts with reduced leakage, lower active currents, and harmonized energy management policies
Development of dedicated microelectronic process options and devices	Improved availability of low-threshold/native/depletion MOSFETs for supporting energy harvesting from ultra-low voltage sources (tens of mV) Improved power switch performance (lower driving voltage, lower leakage, lower on-resistance)	Development of more efficient power switches with low control voltage and negligible leakage (microelectronic, or micromechanical alternatives)
System integration and smart packaging	cm-scale energy autonomous systems	mm-scale energy autonomous systems
Accept high input voltages on microelectronic implementations	Implementations on BCD or CMOS-HV processes	

Definition of FoMs or planned evolution

FoM / Planned Evolution	2023	2026	2029	2033
Minimum 'steady-state' allowed input voltage and power	< 50 mV, < 1 µW	< 38 mV, < 730 nW	< 26 mV, < 460 nW	< 10 mV, < 100 nW
Minimum input voltage and power for cold-start-up	< 100 mV, <1 µW	< 73 mV, < 730 nW	< 46 mV, < 460 nW	< 10 mV, < 100 nW
Minimum Conversion efficiency	70%	73%	76%	80%
Maximum input voltage allowed	20 V	17 V	14 V	10 V

Recommendations for concept 9

- In order to devise mm-scale autonomous systems and dramatic reductions in system size, the recommendations include: Investigate size reduction of inductors; enhancement of efficiency of inductor-less power converter circuit topologies; develop planar alternative to inductors which can be integrated at wafer-level (e.g. MEMS piezoelectric transformers)
- Tune microelectronic process parameters to reduce leakage and to allow lower activation voltages, improve the quality of the switches including also the exploration of low-voltage electromechanical switches.

Application examples

The following table illustrates several industrial application examples in four different scenarios: i) transports (automotive and railroad), ii) industrial and infrastructures monitoring (equipment and pipes), iii) IoT for domotic applications and iv) applications for health, wearables or implantable devices. Several use-case examples are considered in each scenario taking into account ambient conditions to estimate the main FoM for each energy harvesting technology (power density generated when applicable).

With respect to the figures of merit (FoM) reported below, it should be noted that the actual available power for the load also depends on the efficiency of the power management circuitry. For ultra-low power regimes, this is mainly driven by design trade-offs between internal consumption and losses. Reference power conversion efficiencies reported in scientific literature are 40-80%[30] for input power levels up to 10 µW, and increase up to 90% for power levels in the order of 100 µW[31]. Higher efficiencies can be accounted for as input power increases[32].

Like power management circuits, local energy storage devices including microbatteries and microcapacitors, are transversal to the envisaged applications and can be adopted in system architectures. Integration for specific applications will direct the choice of storage materials with, for example, solid-state options being more appropriate for high temperature applications with TEG devices. The presence of such storage devices generally relaxes constraints on energy budgets, which are then based on the overall harvested energy rather than on peak power. Moreover, they can guarantee that a device is enabled even in the absence of sufficient instantaneous power from energy transducers. In any case, energy budgets should account for the fact that every energy transfer from and to energy devices is characterized by a given efficiency, with reference values similar to those listed above for power management circuits.

Application 1: Transports (automotive, railroad)

Example of use-case	Technology	Ambient Conditions	FoM 2023 +5 years	FoM 2026	FoM 2029	FoM 2033 +15 years
Sensor on freight wagon	Outdoor solar (commercial devices c-Si cells)	5000-15000 lux	>23 mW/cm^2	>23.6 mW/cm^2	>24.2 mW/cm^2	>25 mW/cm^2
Sensor near car engine	Thermal Harvesting /small heatsink (~mm thick)	Hot source= 125 °C Cold 60 °C	>250 µW/cm^2	>280 µW/cm^2	>310 µW/cm^2	>350 µW/cm^2
Sensor near car engine	Thermal Harvesting / large heatsink (~cm thick)	Hot source= 125 °C Cold 60 °C	>25 mW/cm^2	>27,4 mW/cm^2	>29,8 mW/cm^2	>33 mW/cm^2
Sensor on truck trailer	Piezoelectricity with mechanical harvesting (Research MEMS)	Freq= 200 Hz Acc= 1 G	>0.6mW/cm^2 (4mW/cm^3)	>0.66mW/cm^2 (4.6mW/cm^3)	>0.72mW/cm^2 (5.2mW/cm^3)	>0.8mW/cm^2 (6mW/cm^3)
	Piezoelectricity with mechanical harvesting (Commercial)		>0.1mW/cm^2	>0.115mW/cm^2	>0.13mW/cm^2	>0.15mW/cm^2
	Miniaturized electromagnetic harvesters		>0.3mW/cm^2 (10mW/cm^3)	>0.36mW/cm^2 (13mW/cm^3)	>0.42mW/cm^2 (16mW/cm^3)	>0.5mW/cm^2 (20mW/cm^3)
	MEMS electromagnetic harvesters		>1µW/cm^2	>3.7µW/cm^2	>6.4µW/cm^2	>10µW/cm^2

Application 2: Industrial & Infrastructures Monitoring (equipment, pipes)

Example of use-case	Technology	Ambient Conditions	FoM 2023 +5 years	FoM 2026	FoM 2029	FoM 2033 +15 years
High voltage busbars temperature monitoring	Indoor photovoltaics	100 lux	>10 µW/cm^2	>10.6 µW/cm^2	>11.2 µW/cm^2	>12 µW/cm^2
High voltage busbars temperature monitoring	Thermal Harvesting on busbars / large heatsink (~cm thick)	Hot source= 45 °C Cold 30°C	>1.3 mW/cm^2	>1.36 mW/cm^2	>1.42 mW/cm^2	>1.5 mW/cm^2
Pump vibrations monitoring	Piezoelectricity with mechanical harvesting (Research MEMS)	Freq= 50 Hz Acc= 0.5 G	>0.15 mW/cm^2 (1 mW/cm^3)	>0.165 mW/cm^2 (1.15 mW/cm^3)	>0.18 mW/cm^2 (1.3 mW/cm^3)	>0.2 mW/cm^2 (1.5 mW/cm^3)
	Piezoelectricity with mechanical harvesting (Commercial)		>0.1 mW/cm^2	>0.115 mW/cm^2	>0.13 mW/cm^2	>0.15 mW/cm^2
	Miniaturized Electromagnetic harvesters		>0.3 mW/cm^2 (10 mW/cm^3)	>0.36 mW/cm^2 (13 mW/cm^3)	>0.42 mW/cm^2 (16 mW/cm^3)	>0.5 mW/cm^2 (20 mW/cm^3)
	MEMS electromagnetic harvesters		>1 µW/cm^2	>3.7 µW/cm^2	>6.4 µW/cm^2	>10 µW/cm^2
District Heating: hot water pipes monitoring	Thermal Harvesting on pipes / large heatsink (~cm thick)	Hot source= 90 °C Cold 50 °C	>10 mW/cm^2	>10,8 mW/cm^2	>11,7 mW/cm^2	>12,8 mW/cm^2

30 W. Jung et al., "A 3nW fully integrated energy harvester based on self-oscillating switched-capacitor DC-DC converter," in 2014 IEEE ISSCC, 2014, pp. 398–399; D. El-Damak and A. Chandrakasan, "A 10 nW-1 uW Power Management IC With Integrated Battery Management and Self-Startup for Energy Harvesting Applications," IEEE J. Solid-State Circuits, vol. 51, no. 4, pp. 943–954, Apr. 2016.

31 S. Bandyopadhyay and A. Chandrakasan, "Platform architecture for solar, thermal, and vibration energy combining with MPPT and single inductor," IEEE J. Solid-State Circuits, vol. 47, no. 9, pp. 2199–2215, 2012; M. Dini et al., "A Nano-current Power Management IC for Multiple Heterogeneous Energy Harvesting Sources," IEEE Trans. Power Electron., vol. 30, no. 10, pp. 5665–5680, 2015.

32 Texas Instruments, "bq25504 Ultra Low-Power Boost Converter with Battery Management for Energy Harvester Applications", data sheet; STMicroelectronics, "SPV1050 Ultralow power energy harvester and battery charger",

Application 3 : IoT for domotic applications

Example of use-case	Technology	Ambient Conditions	FoM 2023 +5 years			FoM 2033 +15 years
Wireless sensors to control heaters, lights, occupancy…	Indoor photovoltaics	150 lux (bedroom)	>15 µW/cm^2	>15.9 µW/cm^2	>16.8 µW/cm^2	>18 µW/cm^2
Wireless sensors to control heaters, lights, occupancy…	Indoor photovoltaics	300 lux (living room)	>30 µW/cm^2	>32.1 µW/cm^2	>34.2 µW/cm^2	>37 µW/cm^2
Sensors for Heat control & Heat Meters	Indoor Thermal Harvesting on Heaters / large heatsink ~cm thick)	Hot source= 45 °C Cold 20 °C	>3.8 mW/cm^2	>4.16 mW/cm^2	>4.52 mW/cm^2	>5 mW/cm^2
Sensors for Heat control & Heat Meters	Indoor Thermal Harvesting on Heaters / small heatsink (~mm thick)	Hot source= 45 °C Cold 20 °C	>37 µW/cm^2	>40.9 µW/cm^2	>44.8 µW/cm^2	>50 µW/cm^2

Application 4: Health / wearables / implantable devices

Example of use-case	Technology	Ambient Conditions	FoM 2023 +5 years			FoM 2033 +15 years
Connected seats/Bed for activity monitoring	Indoor photovoltaics	150 lux	>15 µW/cm^2	>15.9 µW/cm^2	>16.8 µW/cm^2	>18 µW/cm^2
Smart patches (medical)	Indoor photovoltaics	300 lux	>30 µW/cm^2	>32.1 µW/cm^2	>34.2 µW/cm^2	>37 µW/cm^2

Synergies with other topics

Materials and equipment (II.7)

All the energy harvesting concepts covered so far use specific materials (piezoelectric, composites, thermoelectric, semiconductors…), their constraints will depend on the application (low temperature, integration into flexible substrates…) and thus will require different fabrication techniques/equipment.

Heterogeneous integration (II.6)

The integration and packaging of the different components of an autonomous device (sensors, power management systems, energy storage, energy harvesters, antennas…) need to be considered in function of the final application (wearables, IoT…).

Smart sensors (II.3)

The development of low power sensing is compatible with energy harvesting technologies to build self-powered sensors.

Smart energy (II.4)

The commercial availability of GaN FET devices with enhanced-mode characteristic (positive threshold voltage) grown on low-cost 6-in silicon wafers, will made possible the exploitation of GaN technology[33], for large-volume power electronics applications, where such devices are particularly interesting for their high power density in conjunction with the very fast switching characteristics. The latter enable the design of highly efficient power amplifiers for WPT (Wireless Power Transfer) applications[34] [35] (see concept 6: RF energy harvesting/wireless power transfer). Indeed, for an effective design of highly efficient switching mode amplifiers in the MHz and microwave range, a high-power active device technology with fast switching characteristics is needed.

33 C. F. Campbell, A. Balistreri,M. Kao, D. C. Dumka, and J. Hitt, "GaN takes the lead," IEEE Microw. Mag., vol. 13, no. 6, pp. 44–53, Sep. –Oct. 2012.5.

34 "White paper: eGaN FETs for wireless power transfer applications,"EPC, El Segundo, CA, USA, 2013. [Online]. Available: http://epc-co.com/epc/DesignSupport/Applications/WirelessPower.aspx.

35 Florian, C., Mastri, F., Paganelli, R.P., Masotti, D., Costanzo, A., "Theoretical and numerical design of a wireless power transmission link with GaN-based transmitter and adaptivereceiver", (2014) IEEE Transactions on Microwave Theory and Techniques, 62 (4), pp. 931-946.

Recommendations

In general, the development of applications is the key to success for EH. IoT and energy harvesting are application-driven today, so projects should mainly focus on the development of a complete application (from harvesting to the use case). Concerning the concepts covered in this roadmap (vibrational, solar, thermal, RF EH and power management), the improvement of their performance and efficiency is as important as the development of "green" materials, replacing toxic/rare materials used nowadays (lead based piezoelectrics, Bi_2Te_3 for thermoelectrics, rare earth based magnetic material, e.g. NdFeB, for electro-magnetic conversion). The use of nanotechnologies is foreseen to increase the performance of all the concepts in general. Flexible and low cost approaches for wearable applications should be developed as well. Increasing the bandwidth at a low frequency target (below 100 Hz) will help to fit applications for vibration based mechanical energy harvesters. Concerning indoor photovoltaic applications, adapted structures and materials (light intensity and spectra…) should be developed, on the other hand standard procedures for indoor photovoltaic cells characterization should be defined (light intensity and spectra, direct and diffuse light, temperature…). Intentional Far-field RF WPT will exploit the mm-wave band for enhancing rectenna miniaturization and focusing of the energy transfer. Energy storage is required as a hybrid device with the EH options to alleviate any transient effects and assist with higher power operation. Concerning power management circuits, it would be key to investigate size reduction of inductors, to enhance the efficiency of inductor-less power converter circuit topologies, to develop planar alternative to inductors and to tune microelectronic process parameters and technologies to reduce leakage for reduced power consumption and allowing low input voltages.

II.6 System Design and Heterogeneous Integration

Executive summary

Building a roadmap for System Design and Heterogeneous Integration is a tough challenge, because of the variety of applications involved, demanding for very different requirements, sometimes even contrasting in terms of values, limits and importance. Several roadmapping attempts have been done in the past. The first example is the 2007 revision of ITRS[1] where some quantitative Figures of Merit (FoM) were given in terms of percentage of improvement over standards or targets. In the following ITRS revisions of 2009[2] and 2011[3], quantitative FoMs have been replaced by bar charts, related to the topic's development status with respect to the time horizon. By contrast, ITRS 2.0 contained a comprehensive chapter in Heterogeneous Integration, however, focusing exclusively on the technology independent of the application pull[4]. Some more recent efforts discuss the applications in more detail but do not provide a holistic framework to define FoMs within the system application constraints[5].

It is therefore justified to consider a new approach for roadmapping System Design and System Level Applications, which goes beyond the simple inclusion of static numerical tables.

The NEREID approach is to build a general Top-Down description of the requirements[6] (a hierarchical map) that has to be met in a Bottom-Up process, with concepts, methods, values and expectations strictly related to the application of reference.

The Application is the Driver of the System level activities, and so roadmapping has to start from this basic principle as depicted in Fig. II.6.1: Application-driven Methodology, which is explained later.

Relevance

System design and heterogeneous integration are core technology enablers to overcome the challenges arising from the ever increasing complexity of embedded systems, which require to design System on Chips (with integration of digital and analog functions) and systems of SoC with built-in intelligence. Accordingly, every application expert emphasized the importance of system design and heterogeneous integration during all discussions on the different NEREID Workshops.

Competitive value

With respect to other continents, Europe can rely on a huge and original knowledge on system level applications and in More than Moore technologies. Smart Systems are strategic assets present in Europe and so European companies can play a leadership role in the related worldwide market.

It is not only the technologies in Europe that are present, as a result of the ingenuity of a number of device and systems manufacturing companies, the design capabilities at system level are also quite developed. The strong presence of systems in the European industrial and commercial scenario is also confirmed by the fact that international roadmaps (as for example IRDS) are very much less concentrated on systems. This is mainly due to the fact that American and Asian markets are more focused on other technological aspects where they have market advantages.

All of this highlights the importance of Europe working on a systems level roadmap and for European manufacturers and academics to invest resources into pushing this European leadership in Smart Systems and system-level integration knowledge.

Societal benefits

As mentioned above, the strength of systems manufacturing and design in Europe is a reality, bringing the possibility to increase the market presence of European companies in this sector, with a direct impact on the availability of high-value employment jobs across the European community. The creation of high level competences, related to the conception and design of systems, both in system design and at physical level for considering innovative solutions in heterogeneous integration, has a much larger value than to invest in basic knowledge for device production which has become a commodity and requires prohibitive sunk costs of infrastructure for any newcomer.

In systems, knowledge is the key, because the problems and the scenarios relating to where systems are to be applied are very different. This requires strong competences in all the different levels of system design and integration including a solid background of multi-disciplinary understanding. Nowadays heterogeneous integration is playing a fundamental role in productivity and environmental monitoring as well as in health and automotive applications and it is important for Europe to invest in education and system design capabilities. This will provide European workers with the opportunity to become the reference for these aspects on a global scale.

In addition, Smart Systems and system-level integration knowledge can address today's global challenges as they have been captured by the UN Sustainable Development Goals[7]. The deployment of intelligent systems in every day scenarios already demonstrates their potential: to contribute significantly in the reduction of greenhouse gas emissions; to manage the environment and urban development in a sustainable manner; to address food security and safety; to improve the quality of life and healthcare; and to enhance energy and resource efficiency in diverse sectors – from agriculture and the food supply chain, to automotive, mobility and next-generation health services. Examples include environmental monitoring, integrated pest management systems, precision farming, intelligent transportation, advanced driver-assistance systems and self-driving vehicles, energy-efficient buildings, digital manufacturing etc.

Vision

The first step for building the roadmap is to design a structure suitable for having a common (and practical) scheme to be applied and tailored as needed in the different application domains of reference. The basic idea is to consider the functionalities that are of particular interest in future electronic systems. Starting from this consideration, the roadmap structure is built by connecting five different elements of Application-Aware Hardware-Software-Co-Design, as depicted in Fig. II.6.1.

1 International Technology Roadmap for Semiconductors, Design, 2007 Edition

2 International Technology Roadmap for Semiconductors, Design, 2009 Edition

3 International Technology Roadmap for Semiconductors, Design, 2011 Edition

4 ITRS 2.0 'Heterogeneous Integration', 2015 Edition.

5 International Roadmap for Devices and Systems, "Systems and Architectures", 2017 Edition.

6 M. Crepaldi, M. C. Grosso, A. Sassone, S. Gallinaro, S. Rinaudo, M. Poncino, E. Macii, D. Demarchi, "A Top-Down Constraint-Driven Methodology for Smart System Design," IEEE Circuits Syst. Mag., vol. 14, no. 1, pp. 37–57, 2014.

7 https://www.un.org/sustainabledevelopment/

These five elements comprise a list of Functionalities, three kinds of Implementation Qualities (Physicalities, Design Activities and Design Paradigms) and Criticalities and Needs. Some definitions are:

- Functionalities, the reference functions that were identified as the common denominator for System Design and Heterogeneous Integration needs in terms of technology or implementation requests. The identified ones are:
  - Energy Autonomy
  - Connectivity
  - Sensor Integration
  - Miniaturisation
  - Reliability and Life Cycle
  - Functional Safety, Privacy & Security

- The Implementation Qualities are;
  - Design Paradigms, the possible design paradigms useful for serving the functionality needs, evaluated in terms of figure of merit, reporting the importance of the paradigm in solving the functionality needs;
  - Design Tools, useful for implementing the functionality, also evaluated with a figure of merit;
  - Physicalities (i.e. Physical and technological requirements), i.e. the physical implementation requests in terms of heterogeneous technologies and processes;

- Criticalities and Needs are specific challenges within the Implementation Qualities domain that need to be addressed before they become critical bottlenecks for the system level application.

Scope and ambition

From the general roadmap structure that is reported above, the general table has been generated to be used in the specific mapping of the different application domains. The concept, as already highlighted, is that the Application is the core and the starting point of the roadmap. For this reason some important application domains of reference have been selected to which to apply this novel model:

- Automated Driving;
- Implantable Devices;
- Environmental Monitoring and Wearable Systems,

that during the work were identified having very similar requests in terms of roadmapping.

The rationale of choosing these specific applications stems from their importance in European industrial scenarios and from the broad coverage they offer in terms of addressing most of the technology requests useful for building the basis of an effective roadmap.

The aforementioned connection of the five elements is performed by mapping each of the five functionalities to related Implementation Qualities from which specific Criticalities and Needs are derived which results in a roadmap structure, shown in Fig II.6.2.

In practice, starting from the general one, different tables were built, each one referred to one of the three application domains and to one of the functionalities listed above. This results in three times six equals 18 tables. (And as Energy Autonomy is no functionality of Automated Driving it results in 17 tables.)

For each pair of application domain and Functionality the importance of the Functionality for this specific Application domain is indicated (with asterisks, having *** indicating extremely important, * indicating low importance). Furthermore it is indicated the TRL level expected/targeted for that Functionality in that application; both measures are indicated for two time horizons, of more than 5 years (5+) and more than 10 years (10+). In the tables itself …

- the Implementation Qualities are divided in three main implementation targets:
  - Physical and Technological Requirements;
  - Design Methods and Tools;
  - Design Paradigms.
- the Figures of Merits of the Implementation Qualities, in 5+ and 10+ time horizons, are filled in, where possible, with quantitative measures (for example power consumption in nW or time in months/years) and with a qualitative indication where not possible (again with asterisks ***, ** or *);
- the Criticalities and Needs, related to the Implementation Qualities, are also measured in terms of importance in the 5+ and 10+ time horizons.

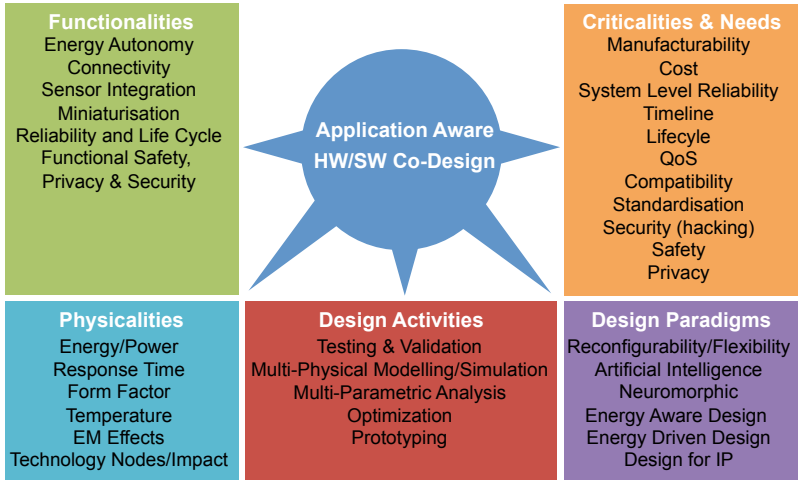

Fig. II.6.1: Application-driven Methodology.

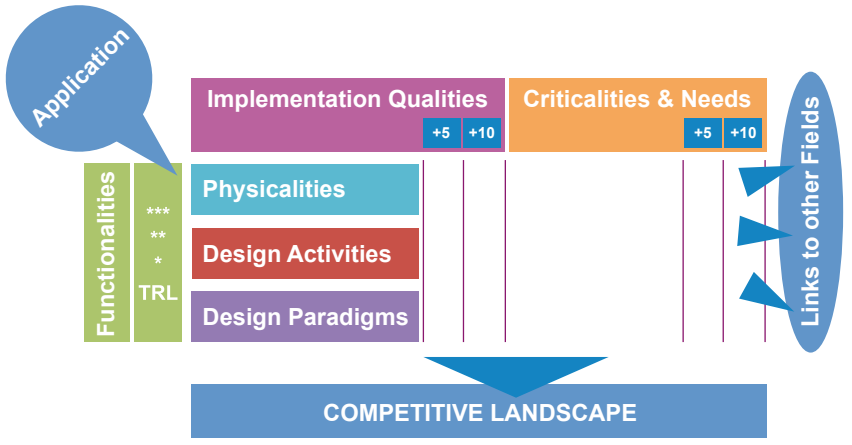

Fig. II.6.2: Some definitions are in order

Mapping into Application Domains

The three application domain roadmaps are reported from Table 1 to Table 17.

Application Domain Automated Driving

"Energy Autonomy", the first functionality under consideration, is decided not to be relevant in the field of automated driving, as it can be assumed, that energy will be available in automated vehicles in the future. This of course does not comprise energy efficiency, which will be relevant. Hence, this table for the application domain automated driving is missing, which results in five tables only for this application.

The functionality "Connectivity" (Table II.6. 1) in the field of automated driving is estimated to be very important (***) in 5+ and also in 10+ years and will have to reach TRL 7 in 5+ and TRL 9 in 10+ years. Table II.6.1 shows the roadmap on implementation qualities and criticalities and needs for Connectivity in the field of automated driving.

Please note, that the links to other workpackes (WPs) inside the tables can be translated to the the chapters of this document in the following way:

- WP2 = II.8
- WP3 = II.1-2
- WP4 = II.3-5
- WP5 = II.6
- WP6 = II.7

Automated Driving Map – Part I on Connectivity

Implementation Qualities: *** = Very Important Quality/Concept

Criticalities & Needs: *** = Very Important to solve/implement it

IMPLEMENTATION QUALITIES	FoM 5+	FoM 10+	Link to other WPs	CRITICALITIES & NEEDS List of Criticalities and/or needs	FoM 5+	FoM 10+
PHYSICAL & TECHNOLOGICAL REQUIREMENTS						
Software (external)	*	*	3		*	*
Software (Internal)	*	*	3	Update over the air (maintenance, security updates, new features)	***	***
Bio-Interfaces	none	none	n.a.	Not applicable		
Speed/Latency	***	***	3	High speed communication (e.g. > 10GB/s;) in the vehicle and for communication of the vehicle to "external" (V2X). Low latency, <= 1ms; real time required for many functions.	***	***
Technology Nodes/Impact on Technology	***	***	2, 3	Accelerated availability of technologies for automotive application; Further decrease of structure size. Early availability of technology support for RF, power etc. which are nowadays supported only delayed (when the base technology is mature).	***	***
Reconfigurability (HW, On-site)	**	**	3	Change of behaviour; Update of hardware capabilities.	*	**
Closed-loop Adaptation	*	*	3		*	*
Communication energy	*	*	3		*	*
New materials for antennas (e.g. CNTs, graphene)	*	*	6,3,2		*	*
New materials for low-loss substrates integrating high-conductivity metal interconnects (e.g., PZT, AIN, porous Si)	*	*	6,3,2	Potential benefit: footprint, size;	*	*
Standardisation	***	***	3	Standardized communication (CAN FD, FlexRay, Ethernet, PON, Bluetooth, 5G) for robust and reliable inter-operability, second source.	***	***
DESIGN METHODS & TOOLS						
Automated Design Space Exploration & System Synthesis	**	**	3	Optimization for speed, latency, gain/noise; Sensitivity analysis	**	***
Verification	**	**	3	Coverage of analog verification; limits	**	***
Constraints for Systems of Systems	**	**	3	Latency; Throughput; Real-time requirements	**	**
Network Verification Tools	**	**	3			
DESIGN PARADIGMS						
Machine Learning Capa-bilities/ Artificial Intelligence	*	*	3	Self-calibration or adaptation for optimal operation (rate, robustness)	*	*
Environment-aware Design	*	*	3	Automotive environment; Real-time requirements	***	***
Open IPs	**	**	3	Standard physical layers and protocols	**	**

Table II.6.1: Automated Driving Map – Part I on Connectivity

Remark: The 10 GB/s in speed is an upper border which is not needed everywhere. Due to high constraints in real time systems such a speed will be necessary in the far future, especially regarding the calculation of radar signals, where pattern recognition will not be sufficient in every case. . If a latency just below 1 ms will be sufficient is pending, now it has been derived from the 5G standard.

The functionality "Sensor Integration" (Table II.6.2) in the field of automated driving is estimated to be very important (***) in 5+ and also in 10+ years and will have to reach TRL 7 in 5+ and TRL 9 in 10+ years. Table II.6.2 shows the roadmap on implementation qualities and criticalities and needs for Sensor Integration in the field of automated driving.

Automated Driving Map – Part II on Sensor Integration

Implementation Qualities: *** = Very Important Quality/Concept

Criticalities & Needs: *** = Very Important to solve/implement it

IMPLEMENTATION QUALITIES	FoM 5+	FoM 10+	Link to other WPs	CRITICALITIES & NEEDS List of Criticalities and/or needs	FoM 5+	FoM 10+
PHYSICAL & TECHNOLOGICAL REQUIREMENTS						
Computing/Storing Capabilities	***	***	4,3,2	Higher computing performance for sensor fusion; Hardware acceleration for specific operations. Increasing memory sizes needed, potentially different memory technologies (MRAM, etc.). Neural networks, neuromorpic computing, i.e. any approach that helps to significantly increase compute capacity and lowers power consumption at the same time.	***	***
Sensor Fusion	***	***	4,3	Reliability of the fusion; Detection of sensor faults (false negatives/positives). Stability of the sensors	***	***
Accuracy and Precision	***	***	4	Depends very much on the function e.g. park assistance vs. Object recognition	***	***
Sensitivity	**	**	4	Depends very much on the function. Robustness against disturbances and environmental influences is required.		
Speed/Latency	**	***	4	Depends very much on the function.		
Bandwidth	*	**	4			
Reconfigurability (HW, On-site)	*	*	4,3	Beam forming; Compensation of+I80 imbalances;	**	**
Closed-loop Adaptation	*	*	4,3			
Calibration	***	***	4,3	Cost of calibration to be reduced. Consider cost of compute power; Calibration has to be available over lifetime	***	***
Standardisation	***	***	4,3	Communication interfaces, power supply(?)	***	***
DESIGN METHODS & TOOLS						
Verification	***	***	4,3	Increasing complexity. Cross domain, cross levels of the system hierarchy, consideration of environment/surrounding.	***	***
Cross Domain Specification	**	**	4	Consideration of the environment (e.g. radar sensitivity on rain; user perception on step width of power steering). Identification and impact of dependencies.	***	***
Automated Design Space Exploration & System Synthesis	**	**	4	System sensitivity, Multi-physics/Cross domain and cross system hierarchy levels	***	***
Multiparametric Analysis	***	***	4	Sensitivity, drift, ageing; identification of dependencies, of the critical parameters and value ranges.	***	***
Constraint Propagation	**	**	4	Propagation across domains and across system hierarchy levels. Identification and impact of dependencies.	**	**
Functional partitioning	**	**	4,3	Combination of differentiated technologies (power vs logic, MEMS).	**	**
DESIGN PARADIGMS						
Machine Learning Capabilities/Artificial Intelligence	***	***	4	Dependable object identification; local intelligence (training external);	***	***
Environment-aware Design	**	**	4	Automotive environment; Real-time requirements; Consider environment conditions for on the fly reconfiguration of the sensor system (e.g. choose different kind of sensor).	**	**
Neuromorphic & Bio-Inspired computing (from energy-driven to survival-driven)	none	none		none		

Table II.6.2: Automated Driving Map – Part II on Sensor Integration

The functionality "Miniaturisation" (Table II.6.3, next page) in the field of automated driving is estimated to be (just) important (**) in 5+ and also in 10+ years and will have to reach TRL 7 in 5+ and TRL 9 in 10+ years. Table II.6.3 shows the roadmap on implementation qualities and criticalities and needs for Miniaturiation in the field of automated driving.

Please note, that the links to other workpackes (WPs) inside the tables can be translated to the the chapters of this document in the following way:

- WP2 = II.8
- WP3 = II.1-2
- WP4 = II.3-5
- WP5 = II.6
- WP6 = II.7

Automated Driving Map – Part III on Miniaturisation

Implementation Qualities: *** = Very Important Quality/Concept

Criticalities & Needs: *** = Very Important to solve/implement it

IMPLEMENTATION QUALITIES				CRITICALITIES & NEEDS		
	FoM 5+	FoM 10+	Link to other WPs	List of Criticalities and/or needs	FoM 5+	FoM 10+
PHYSICAL & TECHNOLOGICAL REQUIREMENTS						
Form factor (size, weight, footprint)	***	***	6,2	Flexible electronics; reduced weight and size under consideration of cost	**	**
Dimensionality	*	*	6	3D integration might be needed for certain functions in order to minimize the size.	*	*
Reconfigurability (HW, On-site)	none	none		Update of capabilities, compensation of imbalances	**	**
Technology Nodes/Impact on Technology	**	**	6,3,2	Accelerated availability of new technologies for automotive. RF capabilities (f_G > 350 GHz(?)); Increased performance (speed), limited losses and parasitics. MEMS.		
System on flex	*	*	6	At affordable cost and with the required robustness Stacking of chips, thin die handling, near memory computing, in-memory computing		
3D (Handling thin die, TSV aspect ratio, inspection tools)	**	**	6			
Biocompatible and invisible sustainable materials	none	none		Not applicable		
Standardisation	*	*	6	Plugs; mounting; Compatible materials	**	**
Transfer printing, 3D additive manufacturing etc.	Defined and detailed in WP6					
Thin and large area electronics including R2R, S2S						
DESIGN METHODS & TOOLS						
Verification	***	***		Complexity, parasitics; Modelling	***	***
Automated Design Space Exploration & System Synthesis	**	**		Partitioning; (consider functional and physical aspects); cross-domain (photonic, electrical, mechanical, thermal, …) Modularity.	**	**
Functional partitioning	**	**		power vs. Logic technologies	**	**
DESIGN PARADIGMS						
Design technology co-optimisation	**	***		Accelerated availability of new technologies for automotive; Early support of "special" features such as RF.	**	**

Table II.6.3: Automated Driving Map – Part III on Miniaturisation

The functionality "Reliability & Lifecycle" (Table II.6.4, on the right) in the field of automated driving is estimated to be (just) important (**) in 5+ and also in 10+ years and will have to reach TRL 7 in 5+ and TRL 9 in 10+ years.

Table II.6.4 shows the roadmap on implementation qualities and criticalities and needs for Reliability and Lifecycle in the field of automated driving.

Automated Driving Map – Part IV on Reliability & Lifecycle

Implementation Qualities: *** = Very Important Quality/Concept

Criticalities & Needs: *** = Very Important to solve/implement it

IMPLEMENTATION QUALITIES			CRITICALITIES & NEEDS		
	FoM 5+	FoM 10+	List of Criticalities and/or needs	FoM 5+	FoM 10+
PHYSICAL & TECHNOLOGICAL REQUIREMENTS					
Assembly for automation	**	**	Testability; (Self-) test in the application;	**	**
Electro-Magnetic Effects	**	**	Victim and disturber perspective.	**	**
Physical robustness	**	**	Vibration; Thermal stress; Humidity and resistance against other chemicals (SO_2)	**	**
Accelerated testing	**	**	Ageing models; relevant parameters for prediction of analog circuitry aging; prediction of time to fail / lifetime; new qualification approaches required due to extended operation times (5x - 15x) at constant or increasing lifetime		
Operating Environment (temperature, humidity, biofouling, corrosion resistance etc.)	**	**	Temperature, humidity, chemicals Protection against humidity; chemicals, corrosion; Physical robustness		
Hermeticity/Insulation	**	**			
Fault tolerance	***	***	Fault detection and recoverability; redundancy; operation time prediction: Spreading of faults	**	**
DESIGN METHODS & TOOLS					
Verification	***	***	Complexity; Cross domain; extended "period of observation"; spreading of faults across the hierarchy;	***	***
Design & Test for Manufacturing	***	***	Complexity;	**	**
Design for Maintainability/Serviceability	***	***	Complexity; Integration vs maintainability; redundancy; HW/SW partitioning; HW updates during lifetime (enhance capabilities; replace defect parts).	*	**
Physics of failure, modelling and virtual testing	***	***	Acceleration models; fault models for enhanced technologies; ageing.	**	**
DESIGN PARADIGMS					
Reusability (system IPs)	***	***	Qualification strategies to minimize re-qualification efforts, time, cost in case of e.g. component updates	**	***
Environment-aware Design	***	***	Automotive requirements. Consideration of operation/environmental conditions on ageing and robustness of operation. Operation time is expected to increase by a factor of 5 to 15 (depending on the function) over the (same) lifetime of 15 years.	***	***

Table II.6.4: Automated Driving Map – Part IV on Reliability & Lifecycle

The functionality "Functional Safety, Privacy & Security" (Table II.6.5) in the field of automated driving is estimated to be very important (***) in 5+ and also in 10+ years and will have to reach TRL 7 in 5+ and TRL 9 in 10+ years. Table II.6.5 shows the roadmap on implementation qualities and criticalities and needs for Functional Safety, Privacy & Security in the field of automated driving.

Automated Driving Map – Part V on Functional Safety, Privacy & Security

Implementation Qualities: *** = Very Important Quality/Concept
Criticalities & Needs: *** = Very Important to solve/implement it

IMPLEMENTATION QUALITIES	FoM 5+	FoM 10+	CRITICALITIES & NEEDS List of Criticalities and/or needs	FoM 5+	FoM 10+
PHYSICAL & TECHNOLOGICAL REQUIREMENTS					
Operating Environment (temperature, humidity, biofouling, corrosion resistance etc.)	*	*			
Electro-Magnetic Effects	***	***	Prevent observations of functions. EMI robustness (high field strengths, spikes, …) against manipulations from outside.	**	**
Physical Robustness	*	*			
Reconfigurability (HW, On-site)	*	*	Update of capabilities; change behaviour;		
Tamper protection	***	***	Hardware based security; End to end security		
Cyber Security incl. data encryption, transfer protocols and data privacy	***	***	Hardware based security; End to end security; encryption, authentication; Security by design.		
DESIGN TOOLS					
Verification	***	***	Injection of faults; Spreading of faults in the system. (KI) Methods to efficiently cover the verification space, in particular for safety critical functions which would require millions of kilometres driving to decrease the remaining risk to an acceptable level.	***	***
Automated Design Space Exploration & System Synthesis	**	**	Optimization across the system hierarchy. System modelling across hierarchies. Safety - security co-design	***	***
DESIGN PARADIGMS					
Reusability	***	***	IP - known good parts; Configurable/scalable parts (in terms of performance, functions)	**	**
Machine Learning Capabilities/ Artificial Intelligence	***	***	Maintain functionality over lifetime; Accountability & Traceability.	***	***
Environment-aware Design	***	***	Harsh environment (EMI, humidity, chemicals temperature, …) to be considered for the design; automotive requirements	**	**

Table II.6.5: Automated Driving Map – Part V on Functional Safety, Privacy & Security

Application Domain Implantable Bio-Systems

The functionality "Energy Autonomy" (Table II.6.6a/b) in the field of implantable Bio-Systems is estimated to be very important (***) in 5+ and also in 10+ years. In 5+ years it will have to reach TRL 5 for more traditional storage (batteries) and TRL 3 (for harvesting energy from the body). In 10+ it will reach TRL 8 for batteries and TRL regarding the generation of energy taken from human body (glucose, mechanical movement, …). Table II.6.6 shows the roadmap on implementation qualities and criticalities and needs for "Energy Autonomy" in the field of implantable Bio-Systems.

Implantable Bio-Systems map - Part I Energy Autonomy

Implementation Qualities: *** = Very Important Quality/Concept
Criticalities & Needs: *** = Very Important to solve/implement it

IMPLEMENTATION QUALITIES	FoM 5+	FoM 10+	Link to other WPs	CRITICALITIES & NEEDS List of Criticalities and/or needs	FoM 5+	FoM 10+
PHYSICAL & TECHNOLOGICAL REQUIREMENTS						
Technology Nodes/Impact on Technology	**	**	2			
Low power electronics	***	***	4	Design and production of ultra-low power electronics (with batteries)	< µW (circuit consump.)	< nW (circuit consump.)
				Design and production of ultra-low power electronics (without batteries)	< mW (circuit consumption)	< 10 µW (circuit consumption)
Energy storage (e.g., solid state)	***	***	4	Duration	> 15 years	> 30 years
				Recycling of the implantable device	*	**
				Recycling of the external supporting electronics (circuit, energy provision, coils, antennas, …), in particular the battery component	***	***
Energy Harvesting (e.g., new materials)	***	***	4	Energy from outside (energy receivers - antennas, coils, ultrasound, …) - Related to the request of the implant	mW/cm3	mW/cm3
				Production of efficient energy from the body	µW/cm3	mW/cm3
Energy/Power efficient algorithms	***	***	4	Implementation of efficient energy-aware HW/SW co-design algorithms	**	***

Table II.6.6a: Implantable Bio-Systems map - Part I Energy Autonomy

IMPLEMENTATION QUALITIES	FoM 5+	FoM 10+	Link to other WPs	CRITICALITIES & NEEDS List of Criticalities and/or needs	FoM 5+	FoM 10+
DESIGN METHODS & TOOLS						
Automated Design Space Exploration & System Synthesis	*	*	4	Implementation of automated tools for exploring optimal solutions for lowering energy consumption	**	***
				Near/Sub Threshold Design Capabilities	**	***
				Focus of System Synthesis for optimising energy consumption	**	**
Verification	***	***	4	Verification of system functionalities in case of not stable or critic energy levels	***	***
Profile of Energy Sources	***	***	4	Design tools for implementing profiling and monitoring of energy sources	***	***
Constraint Propagation	***	***	4	Tools for propagation of constraints deriving from energy sources, considering their impact on system performances/functionalities	***	***
DESIGN PARADIGMS						
Machine Learning Capabilities/Artificial Intelligence	*	*	4	Design for implementing Machine Learning algorithms for optimising power consumption (for example Machine Learning applied in the decision of when and what has to be measured)	*	*
Energy/Power-driven Design (Energy Transparency)	***	***	4	Application of design paradigms where energy and power are the drivers for design choices in terms both of architecture and fabrication technology	***	***
Environment-aware Design	***	***	4	Use of design paradigms that consider in design choices the harsh environment (temperature, humidity, acid/basic environment, biocompatibility, …)	***	***
				Designer Education on new concepts for energy-aware design	***	***
Neuromorphic Computing / Bio-Inspired (from energy-driven to survival-driven)	**	***	2	Design paradigms inspired by biological systems where is applied the balance power consuption/performance. Adaptation of performances for optimising energy/power consumption	***	***

Table II.6.6b: Implantable Bio-Systems map - Part I Energy Autonomy

Reading the table, it is highlighted the difference that has to be considered between systems with batteries or without batteries. In terms of recycling it is also important to mention the difference between the device itself and some critical parts as circuit, coils and antennas.

From Table II.6.6a/b it is evident too the importance of driving the design to consider new solutions for lower energy consumption.

Implantable Bio-Systems map - Part II Connectivity

Implementation Qualities: *** = Very Important Quality/Concept
Criticalities & Needs: *** = Very Important to solve/implement it

The functionality "Connectivity" (Table II.6.7a/b) in the field of implantable Bio-Systems is estimated to be of little importance (*) in 5+ and also in 10+ years. It will reach TRL 6 in 5+ and TRL 8 in 10+ years. Table II.6.7a/b shows the roadmap on implementation qualities and criticalities and needs for Connectivity in the field of implantable Bio-Systems.

Please note, that the links to other workpackes (WPs) inside the tables can be translated to the the chapters of this document in the following way:

- WP2 = II.8
- WP3 = II.1-2
- WP4 = II.3-5
- WP5 = II.6
- WP6 = II.7

IMPLEMENTATION QUALITIES	FoM 5+	FoM 10+	Link to other WPs	CRITICALITIES & NEEDS List of Criticalities and/or needs	FoM 5+	FoM 10+
PHYSICAL & TECHNOLOGICAL REQUIREMENTS						
Software (external)	*	*	3	Software interfaces for external interconnection of the implantable system (protocol, sw control of transmission power, …)	**	**
Software (Internal)	**	**	3	Implementation of optimised embedded software solutions for efficient on-board interconnections (sensor data exchange, data collection and storage, …)	**	**
Bio-Interfaces	***	***	3	Optimisation of electrical interfacing by use of correct materials, geometries and packaging	***	***
Speed/Latency	*	*	3	Speed of measurements and communication of data	kS/s	kS/s
				Latency in data exchange	ms	ms
Technology Nodes/Impact on Technology	*	*	2	Importance of connectivity for technological choices	*	*
Reconfigurability (HW, On-site)	*	*	2	Possibility of on-site HW reconfigurability for changing functionalities and performances	none	none
Closed-loop Adaptation	*	*	3	Adaptation of communication system with a closed-loop methodology	*	*
Communication energy	**	***	3	Consumption per bit (with batteries)	nJ/bit	pJ/bit
				Consumption per bit (without batteries)	pJ/bit	fJ/bit
				Optimisation of communication channel for minimising power consumption	***	***
New materials for antennas (e.g. CNTs, graphene)	**	***	6 & 3	CNTs (biocompatibility issues)	*	*

Table II.6.7a: Implantable Bio-Systems map - Part II Connectivity

IMPLEMENTATION QUALITIES				CRITICALITIES & NEEDS		
	FoM 5+	FoM 10+	Link to other WPs	List of Criticalities and/or needs	FoM 5+	FoM 10+
New materials for low-loss substrates integrating high-conductivity metal interconnects (PZT, AlN, porous Si)	**	***	6 & 3	Graphene	none	none
				PZT (biocompatibility issues)	none	none
				AlN ((biocompatibility issues)	none	none
				Porous Si	none	none
Standardisation	*	*	3	Standardisation of communication protocols for implanted system with external devices	*	**
DESIGN METHODS & TOOLS						
Automated Design Space Exploration & System Synthesis	**	***	3	Tools for helping the designer to integrate communication parts with the rest of electronic system	**	***
Verification	***	***	3			
Constraints for Systems of Systems	n.a.	n.a.	3			
Network Verification Tools	*	**	3	Tools for veriying the reliability of the connetivity	*	**
				Tools for verifying efficiency of the connectivity through tissues	**	***
DESIGN PARADIGMS						
Machine Learning Capabi-li-ties/Artificial Intelligence	*	*	3			
Environment-aware Design	***	***	3	Application of design paradigms for considering the body environment and its characteristics/ parameters	***	***
Open IPs	*	*	3	Use of Open IPs for developing connecting interfaces of the implantable system	none	none

Table II.6.7b: Implantable Bio-Systems map - Part II Connectivity

In the results related to Connectivity it is interesting to analyse that the global importance given to connectivity is low. Discussing among the experts this aspect is reasonable because it does not mean that connectivity is not important, but that it is not an aspect in which it is strategic to invest in the short and longer term. The reason is that technologies for interconnecting, mostly in wireless, are at a state of development enough mature for which to invest in increasing performances and solutions for connectivity is not considered a fundamental issue.

The functionality “Sensor Integration” (Table II.6.8a/b) in the field of implantable Bio-Systems is estimated to be important (**) in 5+ and very important (***) in 10+ years. It will reach TRL 4 in 5+ and in 10+ years. Table II.6.8a/b shows the roadmap on implementation qualities and criticalities and needs for Sensor Integration in the field of implantable Bio-Systems.

Implantable Bio-Systems map - Part III Sensor Integration

Implementation Qualities: *** = Very Important Quality/Concept

Criticalities & Needs: *** = Very Important to solve/implement it

IMPLEMENTATION QUALITIES				CRITICALITIES & NEEDS		
	FoM 5+	FoM 10+	Link to other WPs	List of Criticalities and/or needs	FoM 5+	FoM 10+
PHYSICAL & TECHNOLOGICAL REQUIREM.						
Computing/Storing Capabilities	**	***	4	Computing power	*	*
				Storing capabilities	MB	< 100 MB
Sensor Fusion	***	***	4	Defined and detailed in the Chapter on Smart Sensors		
Accuracy and Precision	***	***	4			
Sensitivity	***	***	4			
Speed/Latency	*	*	4			
Bandwidth	*	*	4			
Reconfigurability (HW, On-site)	*	**	3	In the long term for reconfiguring the implented device for enhancing performances	**	***
Closed-loop Adaptation	**	***	3	Adaptation of sensing measurements related to the changing environment (temperature, pH, …) & Actuation decisions	***	***
Calibration	***	***	3	Calibration to be done at system level, integrating all the components	***	***
Standardisation	**	***	3	Standardisation of sensor interfaces for allowing their use as Ips and qualification for use in the field (FDA)	**	***
DESIGN METHODS & TOOLS						
Verification	***	***	3	Coverage across domains for verifying intra- and inter-domain interactions	***	***
Cross Domain Specification	***	***	3	Cross domain simulation tools	***	***
Automated Design Space Exploration & System Synthesis	*	**	3	Tools for automatising the design of smart and multiple sensors, with their system integration	* (too early, not yet possible)	** (open possibilities due to new standards in sensor design)
Multiparametric Analysis	**	**	3	Designer Education on System Integration and management of Sensor Fusion	**	***
Constraint Propagation	***	***	3			
Functional partitioning	***	***	3			

Table II.6.8a: Implantable Bio-Systems map - Part III Sensor Integration

IMPLEMENTATION QUALITIES				CRITICALITIES & NEEDS		
	FoM 5+	FoM 10+	Link to other WPs	List of Criticalities and/or needs	FoM 5+	FoM 10+
DESIGN PARADIGMS						
Machine Learning Capabilities/Artificial Intelligence	*	*	3	Design for implementing intelligent algorithms for self-adaptation to physical properties of the patient (for example for deciding the best precision and accuracy and/or self-adaptation of thresholds for alarm signal generation)	*	**
				Machine Learning for sensor fusion management	* impl. extern	* impl. extern
Environment-aware Design	***	***	3	Design Paradigms for considering in design process the Environment Compatibility	***	***
Bio-Inspired (from energy-driven to survival-driven)	**	***	2, 3	Implementation of readout circuits for integration inside bio-inspired and neuromorphic systems	**	***

Table II.6.8b: Implantable Bio-Systems map - Part III Sensor Integration

Analysing the indications of Table II.6.8a/b, it emerges that the Computing Power requested is not so critical, but are highlighted from the other side adaptation to environment, the calibration that has to be done at system level and the importance, increasing in the future, for standardisation.

In terms of Design, the consideration of Cross-Domain aspects is highlighted, adding the importance of the Design Paradigms for Environment Compatibility. Machine Learning is not ranked of high relevance, not because it is not important, but because it has to be implemented out of the implantable device. The increasing of the interest for Neuromorphic and Bio-Inspired approaches is mentioned.

The functionality “Miniaturisation” (Table II.6.9a/b) in the field of implantable Bio-Systems is estimated to be very important (***) in 5+ and also in 10+ years and will reach TRL 5 in 5+ and TRL 8 in 10+ years. Table II.9a/b shows the roadmap on implementation qualities and criticalities and needs for Miniaturisation in the field of implantable Bio-Systems.

Please note, that the links to other workpackes (WPs) inside the tables can be translated to the the chapters of this document in the following way:

- WP2 = II.8
- WP3 = II.1-2
- WP4 = II.3-5
- WP5 = II.6
- WP6 = II.7

Implantable Bio-Systems map - Part IV Miniaturization

Implementation Qualities: *** = Very Important Quality/Concept

Criticalities & Needs: *** = Very Important to solve/implement it

IMPLEMENTATION QUALITIES				CRITICALITIES & NEEDS		
	FoM 5+	FoM 10+	Link to other WPs	List of Criticalities and/or needs	FoM 5+	FoM 10+
PHYSICAL & TECHNOLOGICAL REQUIREMENTS						
Form factor (size, weight, footprint)	***	***	6	Miniaturisation for size critical sensor parts	<100 µm	< 50 µm
				Miniaturisation for control, power parts, power supplies (with batteries)	cm	mm
				Miniaturisation for control, power parts, power supplies (without batteries)	mm	10 µm
				Minimisation of weight for lowering impact of the implant	< 10 g	g
				Optimised footprint of the electronic system to be adaptable in body	cm	mm
Dimensionality	***	***	6	Optimisation of 3D dimensionality for lowering impact and increase acceptance	***	***
Reconfigurability (HW, On-site)	*	*				
Technology Nodes/Impact on Technology	***	***	2 & 6	Process variations impact and related design choices	***	***
				Designer Education on impact on design of novel technologies	***	***
System on flex	***	***	6	Fabrication of flexible and biocompatible substrates for hosting the full system	***	***
3D (Handling thin die, TSV aspect ratio, inspection tools)	***	***	6	For compact and flexible devices. Flip chip placement accuracy.	***	***
Biocompatible and invisible sustainable materials	***	***	6	Biocompatibility of the implant	***	***
Standardisation	**	***		Implementation of standard IPs at System Level and bio-compatible packaging	*	**
Transfer printing, 3D additive manufacturing etc.	Details in WP6		6	Details are in the Chapter on Equipment and Manufacturing		
Thin and large area electronics (R2R, S2S)						

Table II.6.9a: Implantable Bio-Systems map - Part IV Miniaturization

IMPLEMENTATION QUALITIES	FoM 5+	FoM 10+	Link to other WPs	CRITICALITIES & NEEDS List of Criticalities and/or needs	FoM 5+	FoM 10+
DESIGN METHODS & TOOLS						
Verification	***	***		Design Rules for Biological Interface, Cross-Domain	***	***
Automated Design Space Exploration & System Synthesis	*	*				
Functional partitioning	**	**				
DESIGN PARADIGMS						
Design technology co-optimisation	***	***		Optimisation for taking in account the biological environment, system level packaging co-design	***	***

Table II.6.8b: Implantable Bio-Systems map - Part III Sensor Integration

IMPLEMENTATION QUALITIES	FoM 5+	FoM 10+	Link to other WPs	CRITICALITIES & NEEDS List of Criticalities and/or needs	FoM 5+	FoM 10+
Assembly for automation	*	*	6			
Electro-Magnetic Effects	*	*				
Physical robustness	***	***		Robustness against body environmental pressures and ageing	***	***
Accelerated testing	***	***		Development of Acceleration Test	***	***
				Consideration of mixed tests at system level (electronics, communication, bio interfaces and chemical/biological reactions)	***	***
Operating Environment (temperature, humidity, biofouling, corrosion resistance etc.)	***	***		Robustness against body environmental pressures and ageing	***	***
Hermeticity/Insulation	***	***		Study of novel biocompatible materials and packaging techniques	***	***
Fault tolerance	***	***		Development of self-diagnosic solutions for failure recovering (fail-safe mode)	***	***
DESIGN METHODS & TOOLS						
Verification	***	***		Verification of long-term stability of components and system level functionalities/ performances	***	***
Design & Test for Manufacturing	**	**				
Design for Maintainability/Serviceability	*** (Serviceability only)	*** (Serviceability only)		Possibility of reconfiguring the implnanted system for recalibration and improving performances	***	***
Physics of failure, modelling and virtual testing	***	***		Tools for automatic implementation of fault tolerant systems	***	***
				Tools for virtual and remote testing of the implanted system, no accessible when installed	**	**
DESIGN PARADIGMS						
Reusability (system IPs)	*	*				
Environment-aware Design	***	***		Novel design paradigms for considering in the design cycle the impact of the environment on reliability and lifecycle of the implanted system	**	***

Miniaturisation it is evident to be a very important issue and Table II.6.9a/b well reports the expected FoMs and the most important optimisations and fabrications aspects that have to be considered.

The functionality “Reliability & Lifecycle” (Table II.6.10) in the field of implantable Bio-Systems is estimated to be very important (***) in 5+ and also in 10+ years. It will reach TRL 7 in 5+ and TRL 9 in 10+ years. Table II.6.10 shows the roadmap on implementation qualities and criticalities and needs for Reliability & Lifecycle in the field of implantable Bio-Systems.

Implantable Bio-Systems map – Part V: Reliability & Lifecycle

Implementation Qualities: *** = Very Important Quality/Concept

Criticalities & Needs: *** = Very Important to solve/implement it

IMPLEMENTATION QUALITIES	FoM 5+	FoM 10+	Link to other WPs	CRITICALITIES & NEEDS List of Criticalities and/or needs	FoM 5+	FoM 10+
PHYSICAL & TECHNOLOGICAL REQUIREMENTS						
				Lifecycle (not relevant for some, very much relevant for others)	> 30 years	> 40 years
				Design of modular systems with respect of the different lifecycle of the parts and the position in body	***	***
				Study of recyclable and/or biodegradable systems	**	***

Table II.6.10: Implantable Bio-Systems map – Part V: Reliability & Lifecycle

The first important FoM reported in Table II.6.10 is the Lifecycle, expected to be >40 years in the long term. The other mentioned aspects are related to modularity, robustness, biocompatibility and failure recovering. For the Design not particular needs are reported, other than the importance of Verification and Reconfiguration of the devices.

The functionality "Functional Safety, Privacy & Security" (Table II.6.11) in the field of automated driving is estimated to be very important (***) in 5+ and also in 10+ years and will have to reach TRL 7 in 5+ and TRL 9 in 10+ years. Table 11 shows the roadmap on implementation qualities and criticalities and needs for Functional Safety, Privacy & Security in the field of automated driving.

From the needs reported in Table II.6.11, the ones that can be mentioned because not standard are the importance of having implantable devices compatible with imaging tools, the need of designing specific and custom parts for security, and the automation of the detection of dangerous conditions.

In the design part are highlighted the importance of intrusion tests and verification of robustness from external attacks, both for data stealing and for system damaging, and the implementation of design tool modules for automatizing the introduction in the system of HW&SW sections dedicated to safety, privacy & security.

Please note, that the links to other workpackes (WPs) inside the tables can be translated to the the chapters of this document in the following way:

- WP2 = II.8
- WP3 = II.1-2
- WP4 = II.3-5
- WP5 = II.6
- WP6 = II.7

Implantable Bio-Systems map – Part VI: Functional Safety, Privacy & Security

Implementation Qualities: *** = Very Important Quality/Concept

Criticalities & Needs: *** = Very Important to solve/implement it

IMPLEMENTATION QUALITIES	FoM 5+	FoM 10+	CRITICALITIES & NEEDS List of Criticalities and/or needs	FoM 5+	FoM 10+
PHYSICAL & TECHNOLOGICAL REQUIREMENTS					
Operating Environment (temperature, humidity, biofouling, corrosion resistance etc.)	***	***	Automatic control systems for detecting dangerous conditions (system failure or hacking)	***	***
Electro-Magnetic Effects	***	***	Implants compatible with high level imaging tools (MRI, XRay, …)	***	***
Physical Robustness	***	***	Mechancal and material robustness for body protection	***	***
Reconfigurability (HW, On-site)	*	*			
Tamper protection	***	***	Implementation of specific system parts (HW and embedded SW) devoted to security	***	***
Cyber Security incl. data encryption, transfer protocols and data privacy	***	***	Designer Education about the needed regulations and precautions for safety, privacy & security	***	***
			Malfuntioning due to hacking activities or unintentional induced reasons	***	***
DESIGN TOOLS					
Verification	***	***	Intrusion tests and verification of robustness from external attacks both for data stealing and for system damaging	***	***
			Designer Education about the needed regulations and precautions for safety, privacy & security	**	**
Automated Design Space Exploration & System Synthesis	*	*	Implementation of design tool modules for automatising the introduction in the system of hw&sw sections dedicated to safety, privacy & security	*	*
DESIGN PARADIGMS					
Reusability	*	*			
Machine Learning Capabilities/Artificial Intelligence	*	*			
Environment-aware Design	***	***	Novel design paradigms for considering in the design cycle the impact of the environment on safety, privacy & security of the implanted system	***	***

Table II.6.11: Implantable Bio-Systems map – Part VI: Functional Safety, Privacy & Security

Application Domain Environmental Monitoring and Wearable Systems

The functionality "Energy Autonomy" (Table II.6.12) in the field of Environmental Monitoring and Wearable Systems is estimated to be very important (***) in 5+ and also in 10+ years. In 5+ years it will have reached TRL 5 and in 10+ years it will reach TRL 8. Table II.6.12 shows the roadmap on implementation qualities and criticalities and needs for "Energy Autonomy" in the field of Environmental Monitoring and Wearable Systems.

Environmental Monitoring and Wearable Systems map - Part I Energy Autonomy

Implementation Qualities: *** = Very Important Quality/Concept

Criticalities & Needs: *** = Very Important to solve/implement it

IMPLEMENTATION QUALITIES				CRITICALITIES & NEEDS		
	FoM 5+	FoM 10+	Link to other WPs	List of Criticalities and/or needs	FoM 5+	FoM 10+
PHYSICAL & TECHNOLOGICAL REQUIREMENTS						
Technology Nodes/ Impact on Technology	**	***	2	High Performance Batteries & Fuel Cells for wearables	**	***
Low power electronics	***	***	4	Design and production of ultra-low power electronic systems	< mw (circuit consumption)	< µw (circuit consumption)
Energy storage (e.g., solid state)	***	***	4	Operational lifetime	> 2 years	> 2 years
				Recyclability	***	***
Energy Harvesting (e.g., new materials)	***	***	4	Production of efficient energy harvesters	mW/cm3	tens of mW/ cm3
Energy/Power efficient algorithms	***	***	4	Implementation of efficient energy-aware HW/SW co-design algorithms	20% reduction in energy requirements	90% reduction in energy requirements
DESIGN METHODS & TOOLS						
Automated Design Space Exploration & System Synthesis	*	*	4	Implementation of automated tools for exploring optimal solutions for lowering energy consumption	Include energy/ power parameters in design tools	Energy minimisation through power optimisation
				Focus of System Synthesis for optimising energy consumption	Component/cell level energy awareness	Automated low-power system design
Verification	***	***	4	Verification of system functionalities in case of not stable or critical energy levels	Energy aware self-test	Energy aware self-test & reporting
Profile of Energy Sources	***	***	4	Design tools for implementing profiling and monitoring of energy sources	Behavioural models for power sources	Inclusion of behavioural power models in design flow
Constraint Propagation	***	***	4	Tools for propagation of constraints deriving from energy sources, considering their impact on system performances/ functionalities	Identification of constraints and their impact	Energy aware software incl. realistic power supply models

Table II.6.12: Environmental Monitoring and Wearable Systems map - Part I Energy Autonomy

IMPLEMENTATION QUALITIES				CRITICALITIES & NEEDS		
	FoM 5+	FoM 10+	Link to other WPs	List of Criticalities and/or needs	FoM 5+	FoM 10+
DESIGN PARADIGMS						
Machine Learning Capabilities/Artificial Intelligence	**	***	4	Design for implementing Machine Learning algorithms for optimising power consumption (for example Machine Learning applied in the decision of when and what has to be measured)	**	***
Energy/Power-driven Design (Energy Transparency)	***	***	4	Application of design paradigms where energy and power are the drivers for design choices in terms both of architecture and fabrication technology	***	***
Environment-aware Design	***	***	4	Use of design paradigms that consider in design choices the environment (temperature, humidity, acid/basic environment, biocompatibility, …)	***	***
				Designer Education on new concepts for energy-aware design	***	***
Neuromorphic Computing / Bio-Inspired (from energy-driven to survival-driven)	**	***	2	Design paradigms inspired by biological systems where is applied the balance power consuption/performance. Adaptation of performances for optimising energy/power consumption	***	***

Please note, that the links to other workpackes (WPs) inside the tables can be translated to the the chapters of this document in the following way:

- WP2 = II.8
- WP3 = II.1-2
- WP4 = II.3-5
- WP5 = II.6
- WP6 = II.7

The functionality "Connectivity" (Table II.6.13) in the field of Environmental Monitoring and Wearable Systems is estimated to be importance (**) in 5+ and also in 10+ years. It will reach TRL 7 in 5+ and TRL 9 in 10+ years. Table II.6.13 shows the roadmap on implementation qualities and criticalities and needs for Connectivity in the field of Environmental Monitoring and Wearable Systems.

Environmental Monitoring and Wearable Systems map - Part II Connectivity

Implementation Qualities: *** = Very Important Quality/Concept

Criticalities & Needs: *** = Very Important to solve/implement

IMPLEMENTATION QUALITIES				CRITICALITIES & NEEDS		
	FoM 5+	FoM 10+	Link to other WPs	List of Criticalities and/or needs	FoM 5+	FoM 10+
PHYSICAL & TECHNOLOGICAL REQUIREMENTS						
Software (external)	***	***	3	Software interfaces for external interconnection of the wearable system (protocol, sw control of transmission power, …)	**	**
Software (Internal)	**	**	3	Implementation of optimised embedded software solutions for efficient on-board interconnections (sensor data exchange, data collection and storage, …)	**	**
Bio-Interfaces	**	***	3	Optimisation of electrical interfacing by use of correct materials, geometries and packaging	***	***
Speed/Latency	*	*	3	Speed of measurements and communication of data	S/s	100 x S/s
				Latency in data exchange	ms	ms
Technology Nodes/Impact on Technology	**	**	2	Importance of connectivity for technological choices	**	***
Reconfigurability (HW, On-site)	*	**	2	Possibility of on-site HW reconfigurability for changing functionalities and performances	*	*
Closed-loop Adaptation	*	*	3			
Communication energy	**	**	3	Consumption per bit	pJ/bit	fJ/bit
				Optimisation of communication channel for minimising power consumption	***	***
New materials for antennas (e.g. CNTs, graphene)	*	**	6 & 3	Performance improvement from new materials	10%	20%
New materials for low-loss substrates integrating high-conductivity metal interconnects (e.g., PZT, AlN, porous Si)	**	**	6 & 3	Area reduction due to new materials	x0.5	x0.1
Standardisation	*	*	3	Standardisation of communication protocols for wearable system with external devices	development of efficient protocols	standardisation
DESIGN METHODS & TOOLS						
Automated Design Space Exploration & System Synthesis	**	***	3	Tools for helping the designer to integrate communication parts with the rest of electronic system	**	***
Verification	***	***	3			
Constraints for Systems of Systems	**	**	3			
Network Verification Tools	*	**	3	Tools for veriying the reliability of the connetivity	*	**
				Tools for veriying efficiency of the connetivity through tissues	**	***
DESIGN PARADIGMS						
Machine Learning Capabilities/Artificial Intelligence	*	*	3	The intelligence of system is, for example, inside the mobile phone connected to the device, so no great intelligence is needed in the device	*	*
Environment-aware Design	***	***	3	Application of design paradigms for considering the on-body and around-the-body environment and its characteristics/parameters	***	***
Open IPs	*	*	3	Use of Open IPs for developing connecting interfaces of the wearable system	none	none

Table II.6.13: Environmental Monitoring and Wearable Systems map - Part II Connectivity

Please note, that the links to other workpackes (WPs) inside the tables can be translated to the the chapters of this document in the following way:

- WP2 = II.8
- WP3 = II.1-2
- WP4 = II.3-5
- WP5 = II.6
- WP6 = II.7

The functionality “Sensor Integration” (Table II.6.14) in the field of Environmental Monitoring and Wearable Systems is estimated to be important (**) in 5+ and very important (***) in 10+ years. It will reach TRL 7 in 5+ and TRL 9 in 10+ years. Table II.6.14 shows the road-map on implementation qualities and criticalities and needs for Sensor Integration in the field of Environmental Monitoring and Wearable Systems.

Environmental Monitoring and Wearable Systems map - Part III Sensor Integration

Implementation Qualities: *** = Very Important Quality/Concept

Criticalities & Needs: *** = Very Important to solve/implement

IMPLEMENTATION QUALITIES	FoM 5+	FoM 10+	Link to other WPs	CRITICALITIES & NEEDS List of Criticalities and/or needs	FoM 5+	FoM 10+
PHYSICAL & TECHNOLOGICAL REQUIREMENTS						
Computing/Storing Capabilities	***	***	3	Computing power	*	*
				Storing capabilities	Gbytes	Tbytes
Sensor Fusion	***	***	3	Integration and packaging	> 3 (e.g., motion, temperature, bio-signal, air quality)	> 5 (e.g., motion, temperature, bio-signal, UV exposure, alcohol levels)
Accuracy and Precision	**	***	4	Defined and detailed in the Chapter on Smart Sensors		
Sensitivity	**	***	4			
Speed/Latency	*	**	4			
Bandwidth	*	**	4			
Reconfigurability (HW, On-site)	**	**	3			
Closed-loop Adaptation	**	***	3	Adaptation of sensing measurements related to the changing environment (temperature, pH, …)	**	***
Calibration	***	***	3	Calibration to be done at system level, integrating all the components	***	***
Standardisation	**	***	3	Standardisation of sensor interfaces for allowing their use as IPs	***	***
DESIGN METHODS & TOOLS						
Verification	***	***	3	Coverage across domains for verifying intra- and inter-domain interactions	***	***
Cross Domain Specification	***	***	3	Cross domain simulation tools	***	***
Automated Design Space Exploration & System Synthesis	*	**	3	Tools for automatising the design of smart and multiple sensors, with their system integration	* (too early, not yet possible)	** (open possibilities due to new standards in sensor design)"
Multiparametric Analysis	**	***	3	Designer Education on System Integration and management of Sensor Fusion	**	***
Constraint Propagation	***	***	3			
Functional partitioning	***	***	3			
DESIGN PARADIGMS						
Machine Learning Capabilities/ Artificial Intelligence	**	**	3	Design for implementing intelligent algorithms for self-adaptation to physical properties of the environment	**	**
Environment-aware Design	***	***	3	Design Paradigms for considering in design process the Environment Compatibility	***	***
Neuromorphic Computing / Bio-Inspired (from energy-driven to survival-driven)	**	***	2, 3	Implementation of efficient readout circuits	**	***

Please note, that the links to other workpackes (WPs) inside the tables can be translated to the the chapters of this document in the following way:

- WP2 = II.8
- WP3 = II.1-2
- WP4 = II.3-5
- WP5 = II.6
- WP6 = II.7

Table II.6.14: Environmental Monitoring and Wearable Systems map - Part III Sensor Integration

The functionality "Miniaturisation" (Table II.6.15) in the field of Environmental Monitoring and Wearable Systems is estimated to be very important (***) in 5+ and also in 10+ years and will reach TRL 6 in 5+ and TRL 9 in 10+ years. Table II.6.15 shows the roadmap on implementation qualities and criticalities and needs for Miniaturisation in the field of Environmental Monitoring and Wearable Systems.

Please note, that the links to other workpackes (WPs) inside the tables can be translated to the the chapters of this document in the following way:

- WP2 = II.8
- WP3 = II.1-2
- WP4 = II.3-5
- WP5 = II.6
- WP6 = II.7

Environmental Monitoring and Wearable Systems map - Part IV Miniaturization

Implementation Qualities: *** = Very Important Quality/Concept

Criticalities & Needs: *** = Very Important to solve/implement

IMPLEMENTATION QUALITIES				CRITICALITIES & NEEDS		
	FoM 5+	FoM 10+	Link to other WPs	List of Criticalities and/or needs	FoM 5+	FoM 10+
PHYSICAL & TECHNOLOGICAL REQUIREMENTS						
Form factor (size, weight, footprint)	***	***	6	Miniaturisation for less invasive devices (size)	cm	cm
				Minimisation of weight for lowering impact	~ 100 g	< 50 g
				Optimised footprint of electronics to be adaptable on body	cm	cm
Dimensionality	**	**	6	Optimisation of 3D dimensionality for lowering impact and increase acceptance, lowering powering and increasing S/N	cm3	mm3
Reconfigurability (HW, On-site)	**	**		Inclusion in the integrated circuit of programmable hardware for allowing remote reconfiguration in case of updates or patches	**	**
Technology Nodes/Impact on Technology	***	***	2, 6	Process variations impact and related design choices	***	***
				Designer Education on impact on design of novel technologies	***	***
System on flex	***	***	6	Fabrication of flexible and recyclable substrates for hosting the full system	***	***
3D (Handling thin die, TSV aspect ratio, inspection tools)	***	***	6	See WP6 for Manufacturing Technology Details. Remaining challenges are in visualisation of interconnections in 3D structure	SAMx-Ray	Other?
Flip chip placement accuracy	***	***	6	At medium throughput levels	µm	<µm
Biocompatible and invisible sustainable materials	*	**	6	Biocompatible, hydrophobic and antimicrobial coatings		
Standardisation	**	***		Implementation of standard IPs at System Level	**	***
Transfer printing, 3D additive manufacturing etc.	Details in WP6			Details are in the Chapter on Equipment and Manufacturing		
Thin and large area electronics including R2R, S2S						
DESIGN METHODS & TOOLS						
Verification	***	***		Tools for layout rules verification considering reduction of pitch/dimensions and appearance of nano-level phenomena both at electrical and at biological level	**	***
Automated Design Space Exploration & System Synthesis	***	***		Implementation of new methodologies and tools for helping design process and integration of different parts	***	***
Functional partitioning	***	***				
DESIGN PARADIGMS						
Design technology co-optimisation	***	***		Development of new paradigms for targeting the optimised integration of the different subsystems in the global system	***	***

Table II.6.15: Environmental Monitoring and Wearable Systems map - Part IV Miniaturization

The functionality "Reliability & Lifecycle" (Table II.6.16a/b) in the field of Environmental Monitoring and Wearable Systems is estimated to be very important (***) in 5+ and also in 10+ years. It will reach TRL 7 in 5+ and TRL 9 in 10+ years. Table II.6.16a/b shows the roadmap on implementation qualities and criticalities and needs for Reliability & Lifecycle in the field of Environmental Monitoring and Wearable Systems.

Environmental Monitoring and Wearable Systems map – Part V: Reliability & Lifecycle

Implementation Qualities: *** = Very Important Quality/Concept

Criticalities & Needs: *** = Very Important to solve/implement

IMPLEMENTATION QUALITIES				CRITICALITIES & NEEDS		
	FoM 5+	FoM 10+	Link to other WPs	List of Criticalities and/or needs	FoM 5+	FoM 10+
PHYSICAL & TECHNOLOGICAL REQUIREMENTS						
				Lifecycle	> 2 years	> 2 years
				Study of recyclable a systems	***	***
Assembly for automation	**	**	6	Package Cost	**	**
Electro-Magnetic Effects	**	***		Victim and disturber perspective.	**	***

Table II.6.16b: Environmental Monitoring and Wearable Systems map – Part V: Reliability & Lifecycle

IMPLEMENTATION QUALITIES				CRITICALITIES & NEEDS		
	FoM 5+	FoM 10+	Link to other WPs	List of Criticalities and/or needs	FoM 5+	FoM 10+
Physical robustness	***	***	6	Robustness to shocks and to bio-fouling	***	***
Accelerated testing	*	**		Consideration of physical tests at system level to evaluate performance over time (electronics, communication, bio interfaces and chemical/biological reactions)	Each separate component needs to exhibit a lifetime prediction > 3 years	Each separate component needs to exhibit a lifetime prediction > 3 years
Operating Environment (temperature, humidity, biofouling, corrosion resistance etc.)	**	***		Emulation of operating conditions on and around the body need to be investigated	***	***
Hermeticity/Insulation	**	***		Study of novel biocompatible materials and packaging techniques such as Teflon, Paralyne, BCB, polyimide, SiNx	**	***
Fault tolerance	**	**		Development of self-diagnosic solutions for failure recovering	Multiple Sensor and polling	Redundancy
DESIGN METHODS & TOOLS						
Verification	**	**		Verification of long-term stability of components and system level functionalities/performances	Standards based Lifetest	Standards based Lifetest
Design & Test for Manufacturing	**	**		Design and test for manufacturing		
Design for Maintainability/ Serviceability	**	**		Design for Maintainability/Serviceability		
Physics of failure, modelling and virtual testing	**	**		Tools for automatic implementation of fault tolerant systems	**	**
				Tools for virtual and remote testing of the wearable system	**	**
DESIGN PARADIGMS						
Reusability (system IPs)	**	***				
Environment-aware Design	***	***		Novel design paradigms for considering the environmental impact in the design cycle of the wearable system	***	***

Table II.6.16b: Environmental Monitoring and Wearable Systems map – Part V: Reliability & Lifecycle

The functionality "Functional Safety, Privacy & Security" (Table II.6.17) in the field of automated driving is estimated to be very important (***) in 5+ and also in 10+ years and will have to reach TRL 7 in 5+ and TRL 9 in 10+ years. Table II.6.17 shows the roadmap on implementation qualities and criticalities and needs for Functional Safety, Privacy & Security in the field of automated driving.

Environmental Monitoring and Wearable Systems map – Part VI: Functional Safety, Privacy & Security

Implementation Qualities: *** = Very Important Quality/Concept

Criticalities & Needs: *** = Very Important to solve/implement

IMPLEMENTATION QUALITIES			CRITICALITIES & NEEDS		
	FoM 5+	FoM 10+	List of Criticalities and/or needs	FoM 5+	FoM 10+
PHYSICAL & TECHNOLOGICAL REQUIREMENTS					
Operating Environment (temperature, humidity, biofouling, corrosion resistance etc.)	*	*	Automatic control systems for detecting dangerous conditions	**	**
Electro-Magnetic Effects	*	*			
Physical Robustness	*	**			
Reconfigurability (HW, On-site)	*	*			
Tamper protection	***	***	Implementation of specific system parts (HW and embedded SW) devoted to security	***	***
Cyber Security incl. data encryption, transfer protocols and data privacy	***	***	Designer Education about the regulations and countermeasures to be applied for implementing safe and secure devices	***	***
DESIGN TOOLS					
Verification	***	***	Intrusion tests and verification of robustness from external attacks both for data stealing and for system damaging	***	***
			Designer Education about the needed regulations and precautions for safety, privacy & security	***	***
Automated Design Space Exploration & System Synthesis	**	**	Implementation of design tool modules for automation the introduction in the system of hw & sw sections dedicated to safety, privacy & security		
DESIGN PARADIGMS					
Reusability	*	*			
Machine Learning Capabilities/Artificial Intelligence	**	***	Improvement of paradigms of elaboration for increasing safety and minimise intrusion (HW/SW co-design)	***	***
Environment-aware Design	***	***	Novel design paradigms for considering the impact of the operating environment on safety, privacy & security of the wearable system	***	***

Table II.6.17: Environmental Monitoring and Wearable Systems map – Part VI: Functional Safety, Privacy & Security

General and summarised results

Considerations about Functionalities

Functionality	Implementation Quality	Score 5+	10+	Tot
Sensor Integration	Sensor Fusion	9	9	18
Sensor Integration	Calibration	9	9	18
Sensor Integration	Verification	9	9	18
Miniaturisation	Form factor (size, weight, footprint)	9	9	18
Miniaturisation	Verification	9	9	18
Reliability & Lifecycle	Environment-aware Design	9	9	18
Functional Safety, Privacy & Security	Tamper protection	9	9	18
Functional Safety, Privacy & Security	Cyber Security incl. data encryption, transfer protocols and data privacy	9	9	18
Functional Safety, Privacy & Security	Verification	9	9	18
Functional Safety, Privacy & Security	Environment-aware Design	9	9	18
Sensor Integration	Computing/Storing Capabilities	8	9	17
Sensor Integration	Accuracy and Precision	8	9	17
Miniaturisation	Design technology co-optimisation	8	9	17
Connectivity	Verification	8	8	16
Sensor Integration	Standardisation	7	9	16
Sensor Integration	Cross Domain Specification	8	8	16
Sensor Integration	Constraint Propagation	8	8	16
Sensor Integration	Functional partitioning	8	8	16
Sensor Integration	Environment-aware Design	8	8	16
Miniaturisation	Technology Nodes/Impact on Technology	8	8	16
Miniaturisation	3D (Handling thin die, TSV aspect ratio, inspection tools)	8	8	16
Reliability & Lifecycle	Physical robustness	8	8	16
Reliability & Lifecycle	Fault tolerance	8	8	16
Reliability & Lifecycle	Verification	8	8	16
Reliability & Lifecycle	Design for Maintainability/Serviceability	8	8	16
Reliability & Lifecycle	Physics of failure, modelling and virtual testing	8	8	16

Table II.6.18: Functionalities and Implementation Qualities ranking

It is interesting to note that certain Functionalities are of significant importance among all the analysed Application domains and there are several Implementation Qualities with high importance pertaining them. Table II.6.18 shows how often certain Functionalities/ Implementation Qualities have been considered as "very important" ("***") in all three application domain roadmaps. These are considered of most significance for future investment as they cross application boundaries. It is clear that in terms of Functionalities, there is a strong system-level requirement for higher integration of sensors in small form factors without compromising reliability and functional safety throughout the system lifecycle.

Functionality	Implementation Qualities Number	Normalised
Sensor Integration	8	2.00
Reliability & Lifecycle	6	1.03
Miniaturisation	5	0.99
Functional Safety, Privacy & Security	4	0.58
Connectivity	1	0.24

Table II.6.19: Functionalities' ranking

To eliminate the dependence on the number of Implementation Qualities present within a Functionality, Table II.6.19 summarises the score rank normalised by the number of Implementation Qualities. Sensor Integration remains the strongest requirement followed by Reliability & Lifecycle and the need to implement in miniaturised systems. It is also noted that results on Energy Autonomy are slightly skewed due to the lack of this functionality in systems for Automated Driving. Energy Autonomy is of relatively higher importance in the field of Implantable Devices and the Environmental Monitoring and Wearable Systems.

Considerations about Implementation Qualities

The analysis of the Implementation Qualities (IQ) is much more complex, and several data have to be cross-checked. However, this work is important for generating the required general information that gives the possibility of extracting specific recommendations. The overall scheme and the structure of the Tables useful for analysing the results obtained during the roadmapping work is depicted in Fig. II.6.3.

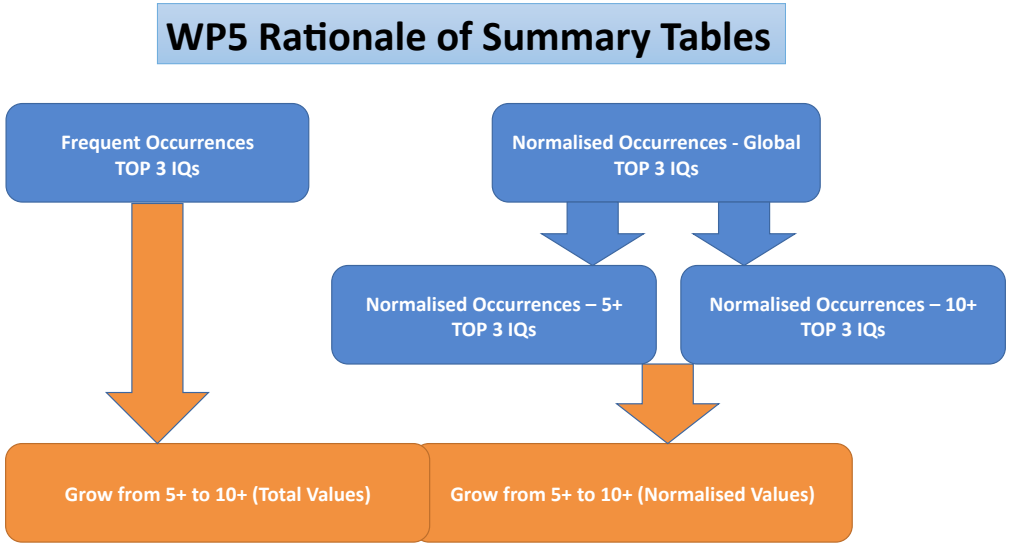

Fig. II.6.3: View of the general result tables

Frequent Occurencies of Implementation Qualities

Table II.6.20: Frequent Occurencies of IQs

Implementation Quality	Occurencies	5+	10+
Verification	98	49	49
Environment-aware Design	78	39	39
Automated Design Space Exploration & System Synthesis	50	23	27
Standardisation	38	17	21
Machine Learning Capabilities/ Artificial Intelligence	38	18	20
Technology Nodes/Impact on Technology	37	18	19
Reconfigurability (HW, On-site)	30	14	16
Functional partitioning	30	15	15
Constraint Propagation	28	14	14
Physical robustness	27	13	14

Table II.6.20 reports the top 10 Implementation Qualities based on their "*" collection ("occurrence") across all application roadmaps. The occurrence indicates their significance independent of Functionality and under any of the Design Paradigms, Design Tools and Physical and Technological requirements headings. It may be of no surprise the Verification is at the top of the list as its contribution is transversal and underlies the development of any Smart System. It is quite interesting that Environment-aware Design (incl. energy considerations) and Automated Design Space Exploration and System Synthesis are also highlighted in the top three Implementation Qualities and have also to be considered of high importance in the future.

Normalised Occurrences of Implementation Qualities

Table II.6.21: Normalised Occurrences of IQs

Implementation Quality	5+	10+	Tot
Calibration	3.00	3.00	3.00
Cyber Security incl. data encryption. transfer protocols and data privacy	3.00	3.00	3.00
Form factor (size, weight, footprint)	3.00	3.00	3.00
Sensor Fusion	3.00	3.00	3.00
Tamper protection	3.00	3.00	3.00
Accuracy and Precision	2.67	3.00	2.83
Computing/Storing Capabilities	2.67	3.00	2.83
Design technology co-optimisation	2.67	3.00	2.83
Verification	2.72	2.72	2.72
3D (Handling thin die, TSV aspect ratio, inspection tools)	2.67	2.67	2.67
Cross Domain Specification	2.67	2.67	2.67
Design for Maintainability/Serviceability	2.67	2.67	2.67
Fault tolerance	2.67	2.67	2.67
Physics of failure, modelling and virtual testing	2.67	2.67	2.67
Environment-aware Design	2.60	2.60	2.60

When the frequency of the Implementation Quality inside the tables is taken out by normalisation, as shown in Table II.6.21, the data reveal further interesting directions (the results are also analysed in the two time horizons, but there are no significant changes in the ranking). In fact some IQs are present in more than one Functionality, so they can collect easier a higher number of "*", obscuring the importance of specific requirements which are less transversal. For example, Verification remains in in position 9 (which corresponds to the 3rd highest score), confirming its importance, but other important IQs emerge. Calibration is considered of top priority along with aspects related to Security and Tamper protection. Sensor Fusion and the Form Factor re-emerge as top priorities mirroring the most important Functionalities derived earlier. Also, to be considered are aspects related to Accuracy and Precision, together with the request of Computing and Storing capabilities and the Co-optimisation of the Design Technology. It is noted that Environment-aware Design also remains in the top five scores.

Grow in the 5+ and 10+ time horizons

Table II.6.22: grow of IQs in 5+ and 10+ time horizons

Implementation Quality	5+	10+	Norm. 5+	Norm. 10+	Global	Normalised
Automated Design Space Exploration & System Synthesis	23	27	1.53	1.80	4	0.27
Neuromorphic Computing / Bio-Inspired (from energy-driven to survival-driven)	8	12	1.33	2.00	4	0.67
Standardisation	17	21	1.89	2.33	4	0.44
Bandwidth	3	5	1.00	1.67	2	0.67
Closed-loop Adaptation	8	10	1.33	1.67	2	0.33
Machine Learning Capabilities/Artificial Intelligence	18	20	1.50	1.67	2	0.17
Network Verification Tools	4	6	1.33	2.00	2	0.67
New materials for antennas (e.g. CNTs, graphene)	4	6	1.33	2.00	2	0.67
Reconfigurability (HW, On-site)	14	16	1.17	1.33	2	0.17
Speed/Latency	9	11	1.50	1.83	2	0.33

Finally, it is worth analysing the "heat map" with emerging topics of interest. Table II.6.22 shows how different IQs pick-up importance in the two different time horizons. The information to be considered is related to the fact that an IQ can be less critical or important in the mid-term but its importance takes over in the longer-term. Here the Automated Design Space Exploration and System Synthesis resurfaces, confirming its importance seen earlier through the analysis of occurrence. It is evident that is considered less critical in the mid-term but it possibly requires more attention as technologies and tools mature. The same it is valid for Neuromorphic and Bio-Inspired approaches which are considered to have a much higher impact in the longer term. The importance of Standardization too will raise, considering probably that the new technologies have to be consolidated and then standardised.

Summary of specific Application Maps

A similar analysis has been performed on the specific Application Maps, organising them as depicted in Figure II.6.4.

The information extracted is not much more elucidating than the analysis above. In fact, looking at the details, priority areas to highlight are linked to the application, of course, and so it is more important to analyse the section "Criticalities & Needs", as done in previous sec-

tions, where there are clear requests to consider for the specific Application domain.

Synergies with other topics

The synergies of the System Design and Heterogeneous Integration chapter with other chapters are natural. System Design and Heterogeneous Integration is on the top of all the other topics collecting their outputs that must be considered for optimising the design and the implementation of heterogeneous integrated systems.

Specifically, the most important interconnections with topics covered in other chapters are:

- With Chapter on "Beyond CMOS" for considering novel approaches in device behaviours, not only related to fabrication, and so with a direct impact on heterogeneous integration, but on design too, where new paradigms have to be considered and implemented in the design-production chain;
- with Chapters on "Advanced Logic" and "Connectivity" the link is stronger on communication side, it was several times mentioned the importance of considering the interconnection (both logical and physical) as a milestone in the design of a system; with Advanced Logic the link is for the realisation of the needed design tools and the integration of the new technological solutions with higher performance at a lower energy cost;
- Chapter on "Functional Diversification" contributes in bringing the issues related to sensors with their integration with readout interfaces and, for example, packaging specifications. The system is nowadays a merge of different technologies and physical domains, analysed in that Chapter;
- Chapter on "Equipment and Manufacturing Science" has the strongest link with the Heterogeneous Integration part, where the needed novel technologies must be brought to an industrial level, studying the manufacturing solutions and the related fabrication equipment.

Recommendations

The activities done inside the System Design and Heterogeneous Integration working group generated the reported tables, but not only. The discussions brought some general recommendations for the future expectations and needs. Summarising all these results together it is possible to conclude that:

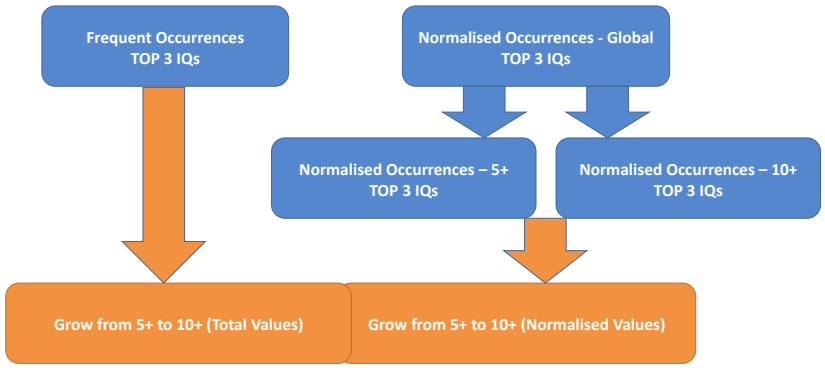

Fig. II.6.4: Rationale of Summary Tables

- Validation is the most requested Implementation Quality across all the Functionalities and Applications. One of the most important related issue is to understand, which is the level of robustness, that is acceptable, its confidence. The question is "When is it done?", so when the validation is considered sufficient? Validation and its approach are a key issue for future system design and implementation;
- The value is not in the device itself, but in system integration and in the related data, the information is at systemic level. This recommendation emerges from the importance given to Sensor Integration and the request of tools for considering the whole system and the interactions (constrain propagation) among the different sub-parts;
- Balance of how much happens at each node and the energy for data transmission (for reliability/security reasons too). Not all the reference applications, as ADAS, consider energy an issue, but in any case the equilibrium of the power consumption among the subsystems is mentioned, in particular for the data transmission;
- Where to position the intelligence it is a design approach that has to be considered for obtaining the functionalities and performances mentioned in the above points above. The right positioning of the intelligence optimises system integration and performances. The future is to move from Embedded Computing to Embedded Intelligence;
- Definition of standards for interoperability. For example in IoT it is mandatory to have the possibility to interact with different other devices. An Open solution can be the right choice, even if openess of standard cannot prevent monetisation.
- Optimisation of Energy is an important part of the expectations, in particular for:
  - System Management;
  - Optimise consumption when is necessary only, highlighting the importance of categorizing the application in terms of Energy Boundaries, giving to designers useful tools for taking in consideration power consumption as part of the design approach and implementation;
- Automated Design Space Exploration and Automated Design Decisions, due to the complexity both in terms of Design and in terms of technology (Heterogeneous Integration of the different parts). It is clear the fact that the systems are moving from Connected Devices to Distributed Embedded Systems, talking of System of Systems). In this scenario Network is a Design Dimension, and Network Synthesis has to be considered in the design flow;
- Environment is Part of the System, it is no more related to the final validation test. For this reason environment is part both of the heterogeneous integration of the system subparts and has to be considered at design level;
- Add Software in the middle, starting from the application. It is clear that software can give to the system enough flexibility and the capability of trimming its performances for reaching all the listed targets. Re-Usability and Reconfigurability are Implementation Qualities that were highlighted in the roadmap tables.

In Europe all the needed competences are present. Several leading companies are engaged in designing and producing systems. For this reason the strategic conclusion is that it is for Europe a very good opportunity to drive an increase in System Knowledge. The many important stakeholders present in Europe can take the opportunity of the emerging profitable system level needs for the future of electronic products, bringing Europe to a leading possibility for System Level Applications.

II.7 Equipment and Manufacturing Science

Executive summary

NEREID's approach to create a comprehensive "Nano-Electronics Roadmap for Europe" is quite a challenge, in particular for II.7, where all other topics of the roadmap, e.g. Beyond CMOS, Nanoscale FET etc., have to be considered from equipment, materials and manufacturing perspective. WP6 - Equipment, Materials and Manufacturing Science is mainly concentrating on equipment and materials but does also reflect manufacturing related things.

The II.7 part of the roadmap was drafted after several consultations with technical experts of II.7 during WP6 domain workshops, by analysing the available information of the other work packages and by reviewing the application-oriented talks presented during the first general workshop, the second general workshop and the presentations given at the cross-domain workshop.

In the context of equipment and manufacturing science no real figures of merits were given, but there are Technology Reediness Level (TRL) indications for the defined NEREID time horizons.

Relevance

Competitive Value

In all the discussions with the II.7 Experts, it was clear that it will not be possible to include real figure of merits (FOMs) for this very broad section of the NEREID roadmap, but the availability and TRL indications are of high value as well.

The timely availability of required equipment and materials provides the suppliers the long-term visibility, which is needed to allocate the R&D investments to guarantee the successful continuation of the nanoelectronics industry in Europe. In fact Europe has a well-established supplier industry for nearly all application markets: More Moore, More-than-More, Heterogeneous Integration etc. The suppliers will take the advantage to initiate R&D work by them or in cooperation with the existing and excellent R&D ecosystem in Europe. But also, European manufactures of ICs, MEMS and smart systems etc. will benefit by this road mapping activity. The topics around manufacturing science will guarantee that the European manufactures stay competitive, even with partly mature facilities.

Societal Benefits

Beside the competitive value of the II.7 roadmap, described in the previous section, there are societal benefits as well. II.7 will contribute to increase the presence of European companies in the field of nanoelectronic and create an impact on the job market, on supplier as well on manufacturer side.

Another benefit given by II.7 is an early consideration of upcoming replacement materials, if there will be national or European regulations. This will be elaborated in the section on manufacturing science in the area of ESH (environment, safety and health).

Vision

Processing tools and high quality materials have been the key enabling factors in the evolution of Nanoelectronics, and in particular in the area of More Moore. The objective of this WP is to extend this benefit to the increased complexity and variety of technologies developed for More-than-Moore but also for nanoscale FET and Beyond CMOS, covered in this WP6 roadmap. A close cooperation was established between device and process developers, on one side, and equipment and materials supplier on the other side.

The scaling down of the MOS transistor has driven the progress in the ICs performance and the cost per function of the devices has dropped accordingly. For complex devices, the decrease of the cost per functions is achieved by the development of derivative options on top of the core processes and the integration of heterogeneous processes. This leads to increasingly complex line management driven by many process generations, multiple products with short life cycle and high variability in terms of demand. The roadmap aims to activate a converging network of experience and competency involving the academic community for the development of new tools and methods for fab productivity needed to increase efficiency in the fab by managing cycle time, advancing equipment and process control and yield enhancement by providing a reference schedule.

Scope and Ambition

The WP6 roadmap is broken down into several concepts:

- More Moore
- More-than-Moore
- Manufacturing Science

And for each of them there will be detailed information listed in the tables of the next section.

Main Concepts

- Concept 1: More Moore
- Concept 2: More-than-Moore
- Concept 3: Manufacturing Science

Concept 1: More Moore

	2023	2026	2029	2033
Conventional technology node semiconductor device & systems (linked to WP3)				
Equipment & Materials for 7 nm node°	TRL 6 - 8			
FinFET implementation >N7 / 12 nm FDx (Strained CMOS) in situ doped RSD (Gen2), dual STI	TRL 4 - 6	TRL 6 - 8		
<N7 horizontal Gate-All-Around NW 10 nm FDx (Gate Last, SAC)	TRL 6 - 8			
Equipment & materials for 5 nm node°	TRL 6 - 8			
<N5 Vertical GAA	TRL 4 - 6		TRL 6 - 8	
Equipment & materials for 3 nm node °	TRL 2 - 4	TRL 4 - 6	TRL 6 - 8	
Equipment & materials for sub 3 nm node °	TRL 2 - 4		TRL 4 - 6	
Technologies				
Si based technology	TRL 6 - 8			
Si(Ge) to Ge	TRL 4 - 6		TRL 6 - 8	
III/V Ci-Intergration with Si	TRL 2 - 4		TRL 4 - 6	TRL 6 - 8
FD-SOI	TRL 4 - 6			TRL 6 - 8
Nanowires	TRL 4 - 6			TRL 6 - 8
3D Sequential	TRL 4 - 6	TRL 6 - 8		
Advanced Surface Passivation / defect passivation (new materials, scaled technologies)	TRL 2 - 4	TRL 4 - 6	TRL 6 - 8	
Interconnects				
Advanced low-k to airgap	TRL 6 - 8			
Cu based (including liner / barrier)	TRL 6 - 8			
Beyond Cu metallization	TRL 2 - 4		TRL 4 - 6	
Material / thin film growth				
Conventional semiconductor technologies	TRL 6 - 8			
2D materials	TRL 4 - 6			TRL 6 - 8
Spin based materials / stacking	TRL 4 - 6	TRL 6 - 8		
Patterning				
Area Selective Deposition	TRL 2 - 4	TRL 4 - 6		TRL 6 - 8
Area Selective Etching	TRL 2 - 4	TRL 4 - 6		TRL 6 - 8
EUVL	TRL 4 - 6	TRL 6 - 8		
DSA based lithography	TRL 4 - 6			
Metrology				
Materials and contamination analysis	TRL 6 - 8			
CD and overlay	TRL 4 - 6			TRL 6 - 8
3D metrology (physical and chemical parameters)	TRL 2 - 4	TRL 4 - 6		TRL 6 - 8
Film thickness	TRL 4 - 6			TRL 6 - 8
Metrology requirements for system integration	TRL 2 - 4	TRL 4 - 6		TRL 6 - 8

	2023	2026	2029	2033
Beyond CMOS & new compute paradigm options down-select and implement (linked to WP2)				
Spin transistors, Steep sub-Vt slope (FeFET, TFET, NEMS) alternative materials: TMD's, others	TRL 2 - 4	TRL 4 - 6		
Neuromorphic and quantum computing	TRL 2 - 4	TRL 4 - 6		
Equipment, Materials, Metrology & inspection for Beyond CMOS & new compute paradigm options				
Tunneling FET (conventional materials)	TRL 2 - 4	TRL 4 - 6		
Tunneling FET (2D materials)	TRL 2 - 4		TRL 4 - 6	
from charge based to spin based	TRL 2 - 4	TRL 4 - 6		
Memory systems incl. new storage architecture for smart systems, IoT and new compute paradigm				
STT- MRAM/ ReRAM/ PCM / other	TRL 4 - 6			

Competitive Situation

The feeling exists that with the worldwide effort on materials, processes and manufacturing in the domain of More Moore, the imminent needs of European application domains is covered – but in certain domains (e.g. lithography equipment) Europe is playing the leading role.

Recommendations

More specific needs in the other NEREID domains (e. g. More-than-Moore) identified.

Concept 2: More-than-Moore

Process technology for the applications (linked to WP4)	2023	2026	2029	2033
Technology platform for integrated application defined sensors, including packaging	TRL 4 - 6			TRL 6 - 8
CMOS integration, compatibility and readout circuit	TRL 2 - 4	TRL 4 - 6		TRL 6 - 8
Multi-parameter sensing	TRL 4 - 6	TRL 6 - 8		
Manufacturability /sensing functionality and micro-pumps	TRL 2 - 4	TRL 4 - 6		TRL 6 - 8
Autonomous sensor systems	TRL 2 - 4	TRL 4 - 6	TRL 6 - 8	
Role of new materials and nanostructures in sensing (vs. Mature CMOS sensors)	TRL 2 - 4	TRL 4 - 6		TRL 6 - 8
System-in-package (SiP) sensors	TRL 4 - 6		TRL 6 - 8	
Energy harvesting	TRL 2 - 4	TRL 4 - 6		TRL 6 - 8
Equipment & Materials for integrated application defined sensors, including packaging	TRL 4 - 6		TRL 6 - 8	
Assembling testing, metrology and calibration	TRL 4 - 6			TRL 6 - 8
Materials and contamination analysis	TRL 4 - 6			TRL 6 - 8
Equipment & Materials for biomedical devices for minimally invasive healthcare	TRL 4 - 6		TRL 6 - 8	
Maturity level	TRL 2 - 4	TRL 4 - 6		TRL 6 - 8
Packaging	TRL 4 - 6		TRL 6 - 8	
Safety / Security	TRL 2 - 4	TRL 4 - 6		TRL 6 - 8
Miniaturization / form factor	TRL 4 - 6		TRL 6 - 8	
Biocompatibility	TRL 4 - 6		TRL 6 - 8	
Enhanced process technology platforms for power electronics, including integration of passive components and packaging	TRL 4 - 6	TRL 6 - 8		
Equipment & Materials for the enablement of the enhanced process technology platforms for power electronics (high power / high Voltage)	TRL 4 - 6	TRL 6 - 8		
Upgrade SiC technologies to larger wafer sizes (150 mm, 200 mm)	TRL 4 - 6	TRL 6 - 8		
Upgrade GaN technologies to larger wafer sizes (150 mm GaN on SiC, …)	TRL 4 - 6	TRL 6 - 8		
Co-integration of GaN with Si CMOS	TRL 2 - 4	TRL 4 - 6		TRL 6 - 8
Other material for More-than-Moore applications (e. g. Ga_2O_3, AlN, diamond)	TRL 2 - 4		TRL 4 - 6	

Heterogeneous System-on-Chip (SoC) Integration (linked to WP5)	2023	2026	2029	2033
Equipment enabling Heterogeneous Integration	TRL 6 - 8			
Innovative materials enabling Heterogeneous Integration (on chip & package level)	TRL 4 - 6		TRL 6 - 8	
Innovative substrates enabling Heterogeneous Integration (system on flex)	TRL 4 - 6			TRL 6 - 8
Specific equipment and materials enabling innovative MTM devices and heterogeneous integration (e. g. 3D handling, flip chip accuracy, etc.)	TRL 4 - 6		TRL 6 - 8	
Equipment & Materials for further miniaturization and higher functional density for MTM	TRL 4 - 6		TRL 6 - 8	
Upgrade MTM technologies to 300 mm wafers and heterogeneous SiP integration	TRL 6 - 8			
Metrology requirements for system integration (3D metrology)	TRL 2 - 4	TRL 4 - 6		TRL 6 - 8
Equipment for Thin and large area electronics	TRL 4 - 6	TRL 6 - 8		
Equipment for transfer printing, 3D additive manufacturing	TRL 4 - 6	TRL 6 - 8		

Competitive Situation

The EU has a very strong international position in the field of More-than-Moore.

Recommendations

Cover activities in WP6 where application wise Europe is leading, but where specific needs for materials, process and manufacturing require continued attention (e.g. SiC, OLED, etc.).

Concept 3: Manufacturing Science

Environment, Safety, Health (ESH)	2023	2026	2029	2033
Replacement materials (e.g. not based on Bi2Te3)	TRL 4 - 6		TRL 6- 8	
Implementation of capabilities for utility reduction, such as support idle mode, improved scheduling and specific communication between host and equipment for energy savings	TRL 4 - 6	TRL 6 - 8		
Productivity				
Improvement of fab productivity (cycle time, percentage NPW wafers, equipment availability, equipment utilization, yield enhancement, etc.)	TRL 4 - 6			
Supply chain integration	TRL 4 - 6		TRL 6 - 8	
Automation				
Smaller lot sizes, mixed lots and single wafer factory operations	TRL 6 - 8			
Upgrade automation, APC and integration of new sensors and hybrid solutions	TRL 4 - 6	TRL 6 - 8		
Control of variability in manufacturing	TRL 4 - 6	TRL 6 - 8		
Advanced diagnostic and decision support systems (supervision, scheduling, agility, augmenting reactive with predictive, big data analytics)	TRL 4 - 6	TRL 6 - 8		
Real-time simulation support for optimized fab operations	TRL 2 - 4	TRL 4 - 6		TRL 6 - 8
Knowledge management (inter fab flows, fast diagnosis)	TRL 4 - 6		TRL 6 - 8	
FICS migration towards distributed architecture BYOD/Apps	TRL 4 - 6		TRL 6 - 8	
Manufacturing data security considerations	TRL 4 - 6	TRL 6 - 8		
Manufacturing technology exploration for functional integration of novel materials (e.g. Graphene, TMD's, FerroElectric, e.a.) Implemented in existing pilot	TRL 2 - 4	TRL 4 - 6		
YIELD				
Advanced diagnostic systems (augmenting reactive with predictive, big data analytics)	TRL 4 - 6	TRL 6 - 8		
Knowledge management (fast diagnosis)	TRL 4 - 6		TRL 6 - 8	

Competitive Situation

There are a lot of standards (e. g. SEMI) on ESH, productivity, and automation for equipment available. Equipment and information systems have to be as compliant as possible.

Recommendations

Continues alignment with corresponding IRDS chapters, mainly More Moore, Factory Integration, Yield and ESH.

Synergies with other topics

The application specific requirements for materials, processes and manufacturing are best covered within the roadmap of the other chapters (II.1-6 and II.8).

Analysis of all other WPs material (presentation etc.) to derive requirements for II.7.

Intensive communication with other WPs for alignment and improvement of the II.7 roadmap.

Recommendations

Concurrent technology areas (II.1-II.6 and II.8) were analyzing their domains in view of the presented applications and derive immediate and long-term requirements in terms of materials, processes and manufacturing needs.

The feeling exists, that with the worldwide effort on materials, processes and manufacturing in the domain of More Moore, the imminent needs of European application domains is covered. However, more specific needs in the other NEREID domains were identified.

In the WP6 roadmap activities were covered, where Europe is leading in terms of materials, processes and manufacturing, but where the demand from application side is stronger outside of Europe (e.g. EUV lithography equipment).

Cover activities in WP6 where application wise Europe is leading, but where specific needs for materials, process and manufacturing require continued attention (e.g. OLED).

Synergies with ITRS/IRDS activities whenever possible, in particular for the section manufacturing science.

General Recommendations

The aim of future research activities in the field of Nanoelectronics is to further develop Europe's S&T excellence to support technology development and innovation and strengthen its competitiveness and market leadership of the related industries. Research and innovations in Nanoelectronics, covering the medium to long-term impacts, are crucial to the European technological leadership in ICT. They are complementary to ECSEL activities mainly devoted to short term applications.

The detailed recommendations for the Nanoelectronic Technologies covered by NEREID were already mentioned above.

II.8 Beyond CMOS

Executive summary

The aim of this Chapter is to survey the potential of the emerging technologies, new state variables and computing paradigms to provide efficient approaches to information processing, either for distributed computation within the expanding IoT or to realise accelerators on top on CMOS platforms to increase the processing speed. The focus is also on more fundamental issues like heat dissipation at nanoscale that has turned out to be the most critical bottleneck in information processing. The topics were discussed thoroughly in the two Beyond CMOS workshops arranged in May 2016 in Helsinki and in May 2017 in Barcelona. The scopes of the workshops were "Non-conventional information processing approaches and devices", focussing on the technology aspects of the emerging information processing methods, and "Designs and architectures for non-conventional information processing" concentrating on investigating the potential of the new technologies for information processing and computing. In addition, the role of System Design an Heterogeneous Integration-tackled in Chapter II.6 in this Roadmap is crucial for the emerging computation paradigms

Relevance

The Beyond CMOS activities represent medium and long-term research. The cutting edge is in the case specific and tailored performance that can enhance the information processing and reduce the power consumption.

Competitive value

The scaling of CMOS devices and circuits is facing a rather fundamental problem arising from dissipation, the so-called "heath death", which has led to the saturation of the clock frequency, to "dark silicon", i.e., idling parts of the chips to reduce heat production, and to multicore processors.[1] This is shifting the paradigm of today's generic data processors towards specific processing units, driven by the needs of applications. This has been recognised also in the IRDS (the follower of the ITRS) White Paper for Beyond CMOS in which, in addition to the new Beyond CMOS devices, the importance of non-von Neumann architectures and alternative information processing paradigms, have been stressed.[2] Furthermore, in the Rebooting the IT Revolution: A Call to Action event, organised in the US by SIA and SRC in September 2015, the shift of focus towards of networked and distributed intelligent sensors and ubiquitous intelligence was stated.[3] The potential solutions to solve the "heat death" problem and reduce the dissipation include the use of new materials like 2D materials in the switches, the use alternative computing paradigms or use different state variables, spins, photons, phonons or mechanical switches, instead of charge. Unfortunately, most of the development takes place still in academic laboratories.

Societal benefits

The development and production of the high-end digital circuits have concentrated to a few factories outside Europe. The European microelectronics industry still relies on production of circuits but the role of MEMS and ASIC applications is growing. This development opens up a possibility to shift the focus to novel intelligent sensing and distributed computation applications, which need a new generation of skilled scientists and engineers for hardware, software, materials and process development. This will then reflect to economy, employment and academic curricula.

1 M. Waldrop, More than Moore, Nature 530 (2016) 144.
2 INTERNATIONAL ROADMAP FOR DEVICES AND SYSTEMS, 2016 EDITION, BEYOND CMOS, https://irds.ieee.org/images/files/pdf/2016_BC.pdf.
3 https://www.semiconductors.org/clientuploads/Resources/RITR%20WEB%20version%20FINAL.pdf.

Vision of Beyond CMOS

Emerging technologies cover a wide range of TRLs from 0-1 to 4-5 with a wide range of device concepts, wide range of materials, some of which are compatible with the current CMOS platform, and novel information processing paradigms in the time frame of five and ten years and further. The aim is to evaluate the potential of the emerging technologies, try to find the strong points and challenges, and shape recommendations for future research. Although the focus is on information processing, the potential of the emerging technologies in sensing has been taken into account. In the long run, it is expected that the new ideas will be taken up more broadly by the academia and, eventually, transferred to industry. There is already currently a relatively strong demand and indirect support to the new approaches in Europe through the existing and forthcoming flagships, focussing on 2D materials, neural networks and quantum technology. Table II.8.1 is listing the categories of Beyond CMOS activities currently supported by the European Research Council, the Future Emerging Technologies and the LEIT ICT programmes of the EC.

Scope and ambition of Beyond CMOS

The scope of Beyond CMOS activities covers several emerging technologies. The target is to identify their potential, challenges and shortcomings when applied in information processing. The emerging technologies mapped in the First Beyond CMOS Workshop included spintronics, neuromorphic computing, heat transport at nanoscale and phononic computing, 2D materials, topological insulators, nano-optomechanics and molecular electronics. Taking into account the maturity of the device technologies, the suitability of the devices for information processing and their integrability, a selection of topics was chosen for discussions in the Second Beyond CMOS Workshop on unconventional computing paradigms. The topics were photonic and nanomechanical computing, computing with spins and magnons, neuromorphic computing, steep-slope devices and statistical/thermal physics and related computing approaches. The tables below, with the main emphasis on information processing, are mainly based on the discussions during the two Beyond CMOS Workshops and the workshop reports produced, and on further discussions with the experts within the NEREID consortium.

Main Concepts

- Steep slope switches: Tunnel FETs
- Neuromorphic circuits and computing
- Spintronics
- Quantum Photonics
- Phonon, Brownian and nano-opto-mechanical computing

Category	Coverage
Quantum computing	Technologies to build qubits and transport information between them, including algorithmic and architecture
Molecular electronics	Solid-state information processing functions built on organic molecules including biomolecules; molecular spintronics
Spintronics	Spin-based electronics and related materials
2D materials	Carbon-based and transition metal dichalcogenides, as well as electronic and spintronic functions based on these
Extended & beyond CMOS	Non mainstream semiconductor transistors, including III-V materials, steep-slope devices, single electron transistors, etc.
Neuromorphic computing	Hardware implementation of neural networks, analogue and digital, architectures and applications

Table II.8.1: Areas of the current EU portfolio on alternative computing. Thermal issues and entropy driven approaches would enrich the palette. (From the presentation of Mr Eric Fribourg-Blanc in the second Beyond CMOS Workshop in May 2017)

Steep slope switches: Tunnel FETs

Today's advanced CMOS technology operates at energies of the order of 10^4 k_BT per binary switching, which gives us up to about four orders of magnitude space for device innovations down to the fundamental limits. The efficiency of computation has doubled roughly every year and a half for more than six decades and the efficiency improvements enabled the creation of portable devices: laptops, smart phones, wireless sensors, and other mobile computing devices. However, this energy efficiency improvement experienced a certain saturation in recent times and is related to scaling down the voltage supply of modern integrated circuits and microprocessors. A current solution to energy efficiency is the parallelism, which resulted in a new generation of multi-core processors in which the frequency is not anymore scaled-up. Instead, the computation is parallelized to achieve the required performance. However, multi-core design is not a universal solution as it might hit the practical limits in terms of a maximum number of cores per processor.

After 2010 the voltage scaling has been quasi-saturated at values close to 0.7-0.8 V. This is due to the fact that conventional CMOS electronics relies on thermal excitation of electrons over a barrier, necessitating an operating voltage many times larger than the thermal voltage, k_BT/q, to maintain a good ON-OFF ratio (>10^5) for a digital switch. Attempts to further scale down the threshold voltage would result in an exponential increase in the off (leakage) current, I_{off}, of at least ten fold for every 60 mV of V_{th} reduction at room temperature (300 K). To address such a fundamental problem, new classes of Steep-Slope Switches have emerged with the main goal to lower the operation voltage and thus the power consumption by their capability to compress the voltage range of the off to on transition due to a steep subthreshold slope. One of the most successful Beyond CMOS switch candidate is the Tunnel FET (TFET), a solid-state semiconductor device designed as a gated p-i-n diode that operates in reverse bias and exploits the quantum-mechanical band-to-band tunneling (BTBT) at one of the junctions. The TFET has as main benefits a very low leakage current and the carrier BTBT injection mechanism, allowing steep sub-thermionic subthreshold slope permitting the operation voltage scaling down to 100 mV (see Fig. II.8.1).

Competitive situation of Tunnel FETs

TFETs are not presently high-speed logic devices, so target applications should exploit low I_{off} for very low power applications. The possible applications scenarios are: (i) more energy efficient hybrid CMOS-Tunnel FET cores for digital computation, (ii) energy efficient neuromorphic design with Tunnel FETs, and, (iii) use of Tunnel FET for low energy computation, analog and sensing applications in the IoT field.

Recommendations for concept Tunnel FETs

There are several technological issues still to be tackled:

- To demonstrate TFETs with combined performance superior to MOSFETs at <0.3 V.
- To develop understanding of the impact of traps and develop design and technology mitigation strategies.
- To study, optimize and implement more technology boosters for TFETs such as negative capacitance and phase change materials for enhanced performance.
- To develop compact models and design tools including hetero-junctions and III-Vs.
- To investigate hybrid CMOS-TFET core design.
- To evaluate performance beyond DC-IV: LG scalability, speed, noise, variability and reliability.
- To establish foundry-level scalable complementary TFET platforms, preferably hybrid wit CMOS.
- To explore TFETs for analog and sensing applications, with potential integration of 2D/2D architectures in BEOL.

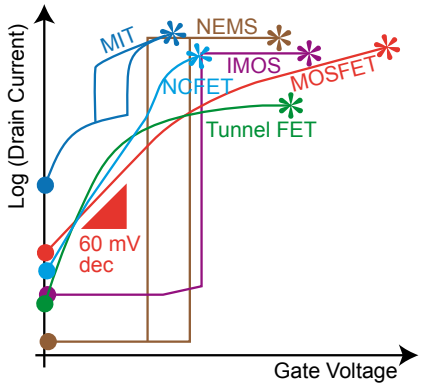

Fig. II.8.1: Various categories of steep slope switches and the positioning of Tunnel FETs in terms of Ioff, Ion and the steepness of the off to on transition, with benefits for low power applications (Courtesy of Prof. Adrian Ionescu, EPFL).

Tunnel FETs

Key research questions/issues

	Medium Term	Long Term
What performance (I_{on}, I_{off}, g_m, SS, switching speed) can be achieved in different materials and geometries? Channel length scalability is likely worse than for MOSFETs, how will this impact applicability for future nodes? Will we be able to bring trap level densities low enough for BTBT to dominate in entire swing region. Origin of trap mechanisms, extrinsic like Dit in the gate stack or intrinsic related to doping tails or material composition, and to which extent can they be controlled. Investigations of variability and reliability of TFETs is still very limited. Boosting of Tunnel FET by disruptive solutions: phase change materials and negative capacitance.	Long-term scalability for TFETs could be an issue, if the gate lengths cannot be scaled because of direct source-to-drain tunnelling and the need for underlapped regions. Traditional scaling should be re-defined in the 2D/2D Tunnel FET architectures. Performance/speed trade-off compared to other advanced devices (NWs, 2D). The goal is to achieve Complementary Tunnel FETs with V_{th} ~0.1 V and V_{dd} ~0.2–0.3 V and I_{on} ~200–500 uA/um. Beyond traditional logic design with Tunnel FETs, such as neuromorphic ICs.	Long-term scalability for the TFETs could be an issue, if gate lengths cannot be scaled because of direct source-to-drain tunneling and the need for underlapped regions. Traditional scaling should be re-defined in 2D/2D Tunnel FET architectures. Performance/speed trade-off compared to other advanced devices (NWs, 2D) The goal is to achieve Complementary Tunnel FETs with V_{th} ~0.1V and V_{dd} ~0.2–0.3 V and I_{on} ~200–500 uA/um. Beyond traditional logic design with Tunnel FETs, such as neuromorphic ICs.

Application needs & Impact for Europe

	Medium Term	Long Term
TFETs are not high speed devices (comparatively), so the target applications should exploit the low I_{off}. Very strong European efforts on TFET both in terms of device technology and simulation. A high potential of Tunnel FETs is the analog gain at low current/voltage and their thermal stability	IoT and other applications targeting lower frequency ranges < 500 MHz – 1 GHz, but where active and passive power consumption is essential. Potentially hybrid technologies mixing TFETs and conventional devices Low power analog ICs with high temperature stability Tunnel FET sensors and new readout interfaces for sub-100 nA current levels	Heterogeneous systems. Complex III-Vs required for TFETs ⇒ potential for co-integration with active photonics, sensing and RF technologies. Exploiting temperature independence of TFETs (once the trap issues are solved), applications with greater temperature span.

Technology and design challenges

	Medium Term	Long Term
Non-standard Si CMOS, requires an ecosystem for III-V capability and integration opportunities. Complementary tunnel FET in other than Si technologies are technologically very challenging. No design infrastructure for TFETs. Reliable TCAD, compact models and design tools, which accurately capture the behaviour and does not require extensive tuning, are needed to enable VLSI TFET designs. Demonstration of vdW Tunnel FET in 2D/2D embodiments for sensing and analog functions	Demonstration of sufficiently good p-and n-TFETs in independent technologies. Demonstration of working devices based on other concepts EHBT-FET, superlattice FET, resonant TFET, 2D/2D tunnel FETs Strong coupling to other technology developments, if III-V MOSFETs do not make it for 7 or 5 nm nodes, TFETs most likely will not either. vdW 2D TFETs, does this technology offer advantages over compound semiconductor technology?	Current best devices are based either on exotic air-bridge/MBE structures or vertical NWs which rely on processing tuned to specific material combinations. For TFETs to become mainstream mature technologies (lateral or vertical) must be developed which allow for complementary TFET circuits. High-performance complementary TFET technologies in foundry environment. 2D/2D Tunnel FETs in BEOL embodiments for smart sensing

Definition of FoMs or planned evolution

	2023	2029
I_{off}, I_{60}, I_{on}, SS_{ave}, g_m Temperature sensitivity included as metric/evalaution Common definition of metrics for comparison of different sources and technologies. I_{60} is an excellent FoM which has been pioneered by simulation. Will become relevant when experimental devices get better. Abolish the use of SS_{min} – meaningless number	Target I_{60} close to 100 uA/um combined with SS_{ave} < 60 mV/dec.	Metrics will be application specific Target I_{60}= 500 uA/um combined with SS_{ave} < 50 mV/dec. Need to demonstrate reasonable dynamic performance, ~1 GHz operation

Other issues and challenges

	2023	2029
Electrostatics more important than for MOSFETs ⇒ need for confined geometries Potential high process variability and sensitivity to process variations; robust design for Tunnel FETs.	Simple correlation of material parameters (μ, m_{eff}, E_G) to device models incorporating heterostructures.	High-performance TFETs will need III-V ⇒ potential synergy with integrated photonics. Analog ICs and sensors based on Ge/SOI Tunnel FETs or on 2D/2D Tunnel FETs in BEOL

Neuromorphic circuits and computing

In neuromorphic computing, electronic circuits mimic the operation of neurons and their architectures to enhance the computational efficiency and reduce the power consumption. The circuits can be digital, analog or mixed, and combined with memory cells. An alternative way is to exploit high performance computing (HPC) with algorithms that emulate, for example, human information processing. Typically, the focus is on specific problems such as pattern recognition like image, speech, text, handwriting as well as data mining. For example, text recognition at 20 pages per second has been demonstrated by a 500 TFLOPS HPC system.[4] Neuromorphic circuits use non-von Neumann architecture and can be realised by integrating a non-volatile memory cell as the synapse with CMOS circuitry representing the neuron.[5] Recently photonic synapses based on phase-change materials were also demonstrated.[6] The circuits can exhibit machine learning to perform, e.g., pattern recognition. Supervised learning is based on repetition of numerous samples,[7] and unsupervised learning needs a few presentation to master the function.[8] The latter is in many cases based on spike timing dependent plasticity (STDP) of the artificial synapses. The hardware realisations make use of combining high-end VLSI CMOS technology and multistate probabilistic memristor synapse systems to create efficient neuromorphic architectures.[9] The unsupervised neural circuits can also be connected to living entities and, in the future, help to construct more efficient, partially artificial, implants.[10] The human brain consumes power in the range of 10-20 W, which is orders of magnitudes less than the power consumption projected for an equivalent system using current technology. However, sub-fJ operation per bit has been predicted in phase change material synapses integrated with carbon nanotubes, showing that there is room to improve the energy efficiency.[11]

Competitive situation of Neuromorphics

Outside Europe, the main player is industry, including both micro/nanoelectronics companies like IBM, Microsoft and Apple and companies providing services and applications, such as Google, Facebook, Baidu and Amazon. It seems that the R&D in Europe is currently split between the Human Brain Project[12] and a series of few research projects on neuromorphic chips and their applications as well as on reservoir computing, funded by the European Commission. While the micro/nanoelectronics companies develop dedicated devices and circuits for neural networks, the service providers exploit the HPC.

Recommendations for Concept Neuromorphics

Neuromorphic computing can benefit from the investments to HPC in Europe. For IoT applications, sensing and automotive industry, development of case specific fast and low power hardware together with the software and interfaces to digital world could turn out to become a new avenue to European electronics, materials and equipment industry. The position of Europe on the map of neuromorphic computing was thoroughly discussed in the Workshop on the Exploitation of Neuromorphic Computing Technologies, held in Brussels in February 2017, and in the followed report.[13]

Medium Term [+5 years]

Long Term [+10 years]

Key research questions/issues

- Neuromorphic components mimic the operation of natural neurons.
- At the device level this means combining analog, or multi-level, and digital information processing, combining memory and switches to realise synapses and produce the corresponding algorithms and circuit architectures to make use of the circuitry.
- Not based on von Neumann architecture and necessarily not on Boolean logic.
- HPC and specific algorithms to emulate the neurons and biological systems.
- One of the key issues is to understand the information processing of biological entities.

Application needs & Impact for Europe

- Pattern recognition including image processing, audio processing, tactile processing, olfactory processing, multisensory integration, EEG and MEG signal processing, medical monitoring (ECG, blood pressure…), brain-computer interfaces, robotics and motor control, financial markets etc.
- Artificial intelligence- and IoT-related approaches to efficient next generation production offer new possibilities to European industry.
- Main activities in development of neuromorphic applications are currently developed outside Europe (including Google, Facebook, Baidu and Amazon, IBM, Microsoft and Apple).

Technology and design challenges

- Dedicated hardware realizations.
- New devices/circuits, which combine memory and decision-making, are mixed analog and digital and can communicate with the digital world are needed.
- The circuits will be in most cases dedicated to specific tasks, and algorithms and interfacing with generic data processing need development.
- Algorithms for HPC environment.

Definition of FoMs or planned evolution

Large variety of technologies and applications at different maturity levels, consequently the FOMs are highly case specific (number of neurons and synapses, energy, speed, pattern complexity, efficiency of learning, etc.)

Other issues and challenges

- Materials and technology development need resources.
- The most efficient approaches rely on hardware dedicated to neuromorphic computing.
- Emulation using HPC, algorithms and interfacing to big data and user interfaces require R&D.
- Links to II.6 System Design and Heterogeneous Integration and II.7 Equipment and Manufacturing Science are relevant.

4 Q. Qiu et al., A Parallel Neuromorphic Text Recognition System and Its Implementation on a Heterogeneous High-Performance Computing Cluster, IEEE Trans. on Computers 62 (2013) 898.
5 G. W. Burr et al., Neuromorphic computing using non-volatile memory, Advances in Physics: X 2 (2017) 89.
6 Z. Cheng et al., On-chip phase-change photonic memory and computing, Proc. SPIE 10345 (2017) 1034519.
7 M. Schmuker, T. Pfeil, and M. P. Nawrot, A neuromorphic network for generic multivariate data classification, PNAS 111 (2014) 2018.
8 T. Masquelier, R. Guyonneau and S.J. Thorpe, Spike Timing Dependent Plasticity Finds the Start of Repeating Patterns in Continuous Spike Trains, PLoS One 3 (2008) e1377.
9 G. Indiveri et al., Integration of nanoscale memristor synapses in neuromorphic computing architectures, Nanotechnology 24 (2013) 384010.
10 T. Werner et al., Spiking neural networks based on OxRAM synapses for real-time unsupervised spike sorting, Frontiers in Neuroscience 10 (2016) 1.
11 F. Xiong et al., Low-Power Switching of Phase-Change Materials with Carbon Nanotube Electrodes, Science 322 (2011) 568.
12 https://www.humanbrainproject.eu/en/.
13 https://ec.europa.eu/digital-single-market/en/news/workshop-exploitation-neuromorphic-computing-technologies.

Spintronics

Spintronics[14] has several aspects related to information technology, since spins can be seen as an extra degree of freedom combined with charge.[15] Examples are spin FETs[16] and spin valve devices.[17] Pure spin currents manifest themselves in, e.g., the spin Hall effect, which can be exploited in microwave oscillators[18] and, potentially, in neuromorphic systems.[19] Spin waves in magnetic insulators, arising from coupled precession of magnetic moments, can transfer information without moving charges and, consequently, without Joule heating or dissipation. Spinwaves, or magnons when quantized,[20] can propagate at wavelengths down to nm and frequencies up to THz. Spin waves with frequencies up to a few tens of GHz can be generated using nano-contact spin torque oscillators. The frequency can be tuned by the driving DC current and with the external magnetic field in a wide range, enabling fabrication of broadband oscillators. Directed spin wave beams can be generated by tilting the external magnetic field, making it possible to couple multiple oscillators and lock them into the same frequency. The distance between the oscillators can be more than 1 µm. The spin Hall effect can also be used to generate oscillations and propagating spin waves in nanoscale constrictions with a small driving current, less than 1 mA. Spin Hall nano-oscillators are relatively easy to fabricate, can be synchronised at large distances and the coupled oscillators can potentially form neural networks for neuromorphic computing. Spintronics has been exploited in hard disk drives and MRAMs already for years. Spin waves and magnons provide new possibilities to information processing, potentially at low power and with fewer devices compared to current CMOS circuits.[21] Most of the fabrication processes are CMOS-compatible. Various components for logics have been demonstrated, including, e.g., switches, transistors and XNOR and majority gates. In addition, it was shown recently that 2D magnetic insulators can be integrated with other 2D materials to build spin filters, memories and potentially spin logic devices.[22] In topological insulators the bulk, whether 2D or 3D, is an insulator but the strong spin-orbit coupling creates a metallic surface state through which spin up or down carriers can propagate without scattering. The state resembles the edge states of quantum Hall effect but without an external magnetic field. The mobility is very high since no scattering takes place, thus facilitating fast interconnections. The resistance is determined by the resistance quantum of 25.8 kΩ, such a resistance is smaller than that estimated for 3-µm long copper interconnects in the 10-nm technology node[23] and can be further decreased in multilayer structures comprising multiple edge states connected in parallel. Strong spin-orbit coupling can be found in heavy elements and their compounds, such as tellurides and selenides. Although the topological states are highly inactive, the interaction with the bulk and with external stimuli, such as photons or magnetic fields, remains open to further studies. Unique properties of topological insulators can be exploited in THz ballistic transistors, reconfigurable interconnects, quantum metrology, and topologically protected quantum computation.

14 I. Zutic, J. Fabian, and S. Das Sarma, Spintronics: Fundamentals and applications, Rev. Mod. Phys. 76 (2004) 323.
15 S. A. Wolf et al., Spintronics: A Spin-Based Electronics Vision for the Future, Science 294 (2001) 1488.
16 S. Datta and B. Das, Electronic analogue of the electro-optlc modulator, Appl. Phys. Lett. 56 (1990) 665.
17 R. Jansen, The spin-valve transistor: a review and outlook, J. Phys. D: Appl. Phys. 36 (2003) R289.
18 T. Chen et al., Spin-Torque and Spin-Hall Nano-Oscillators, Proc. IEEE 104 (2016) 1919.
19 J. Torrejon et al., Neuromorphic computing with nanoscale spintronic oscillators, Nature 547 (2017) 428.
20 S. Neusser and D. Grundler, Magnonics: Spin Waves on the Nanoscale, Adv. Mater. 21 (2009) 2927.

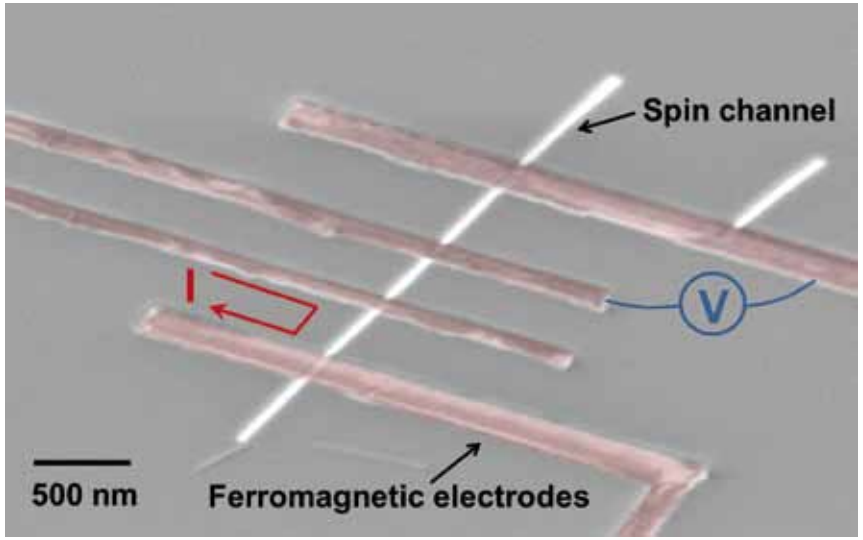

Fig. II.8.2: SEM image of a spin-valve device. A current of a few µA flows between the first two ferromagnetic electrodes. Voltage arising from the pure spin-current is measured between the last two electrodes. This is the non-local configuration, where the charge and spin currents are separated (Courtesy of Dr. Marius Costache, ICN2).

21 T. Fischer et al., Experimental prototype of a spin-wave majority gate, Appl. Phys. Lett. (2017) 152401.
22 S. O. Valenzuela and S. Roche, A barrier to spin filters, Nat. Electron. 1 (2018) 238.
23 Electrical and optical devices incorporating topological materials including topological insulators, Patent US20120138887A1.

Competitive situation of concept Spintronics

The US Department of Energy recently funded a spin-based research cluster called "SHINES" (Spins and Heat in Nanoscale Electronic Systems)[24] consisting of 14 research groups from seven institutes in the country. From the academic point of view it can be argued that Europe, and specially France, leads the spintronic revolution. Germany included in its priory program SPINCAT: "Spin Caloric Transport" (2011-2017) and there is another priority program of the German Research Society (DFG) entitled "Skyrmionics: Topological Spin Phenomena in Real-Space for Applications". At European level, the community of spintronics started its consolidation process led by France and formed in 2016 the network SpinTronicFactory.[25] Its mission is to promote research and innovation in Europe based on spintronics. Spintronics technology was born in Europe, as testified by the Nobel Prize 2007 laureates Profs A. Fert and P. Gründberg, and the participation of academia is very large with a strong global position. However, the participation of industry in spin-based memories, which is the main proven technology so far, is low and, in some aspects of spintronics, almost inexistent. Nevertheless, several European start-up companies focussed on sensor technology have appeared in the last few years, for example, Crocus, Evaderis, Antalos, Capres, Singulus, NanOsc and Elliptika.

5.3.2 Recommendations for Spintronics

Stronger industry-academia interactions are needed to identify jointly solutions to challenges for uptake. The medium-term activity to implement spin torque devices in information processing technology will still need support from national and European stakeholders. In the long term, fruitful interaction of spintronics with the emerging field of topological structures and devices is foreseen.

24 https://science.energy.gov/bes/efrc/centers/shines/.
25 http://magnetism.eu/88-the-spintronicfactory-stf-.htm.

Spintronics

Medium Term [+5 years]

Long Term [+10 years]

Key research questions/issues

- STT-MRAM is ready for volume production.
- Provides reduction of the power consumption.
- Lowering the critical current for writing.
- Spinwaves/Magnonics: Wavelength down to nm and frequency up to THz, 300 K operation and long propagation length (~ cm).
- Compatibility with waveguide concept.
- No Joule heating involved.
- Not fully compatible with CMOS.
- Enhancement of existing launching/detecting techniques required.
- Topological insulators can provide robust interconnects.

Application needs & Impact for Europe

- STT-MRAM is expected to fully seize the e-FLASH technology in the next few years.
- MRAM usual applications are non-volatile operations, memories, memristors, sensors, bioapplications and energy harvesting.
- Magnonics: Potential for computation operation, energy harvesting (spin Seebeck effect), microwave oscillators, memories among many others.
- Size and power consumption reduction.

Technology and design challenges

- Spin wave majority gate and other components exist for logics.
- Reduce the temperature dependence of magnetic anisotropy for high T operation.
- Reduce the size, time of operations and the power.
- Slow group velocity, 10-20 km/s.
- High attenuation (six orders of magnitude higher than for photons in a standard optical fibre).
- Fabrication processes, size and reliability.
- Expensive materials and difficult to grown (YIG).

Definition of FoMs or planned evolution

	2023	2029	2033
Spin wave/magnonics technology is at early stage, performance is material and fabrication tolerances dependent, consequently FOMs are difficult to define.			1-10 aJ
Energy per operation1 (depends on technology)	0.1-1 fJ		
Complexity of circuits	Simple logic operations	Small scale IC	300 K
Topological insulators, operation temperature	77 K		

Other issues and challenges

New materials, equipment and processing technology required (WP5 Equipment and Manufacturing science).

Quantum Photonics

Quantum photonics is selected to illustrate quantum technologies which, according to the Quantum Manifesto[26] on which the recent Quantum Technology flagship in Europe is based, are becoming a new way to look at the world characterised by "objects [that] can be in different states at the same time (superposition) and can be deeply connected without any direct physical interaction (entanglement)".[24] Four quantum technologies areas have been identified so far, namely, Communications, Simulators, Sensors & Metrology and Computing. An implementation plan to roll out the flagship has been worked out[27] and is being followed.

In quantum communications and computation the state variable associated with the information is no longer a digital bit in the classical sense but the quantum bit or qubit, defined as a two-state quantum mechanical system.

Quantum photonics plays a key role in quantum repeaters, since the long-distance transport of qubits is via photons. Quantum simulators will be used for modelling, designing and understanding materials with inherent quantum phenomena. Quantum sensors and metrology are based on superposition while quantum imaging methods rely mainly on entanglement. Quantum computing is seen as the area that will take well over 20 years or more to bear fruits. A huge progress has been made since the days of "optical computation" of the early 1980s, with its optical table-scale and cm-sized components, a progress enabled by silicon technology and the advances in the understanding of, e.g., confined photons and optical resonators. Europe has a strong base in silicon photonics coming from the work on Si-based photonic crystals which, coupled to the long tradition in III-V semiconductor optoelectronics, combines into a Si-based platform that can sustain Si and III-V photonics for a myriad of quantum technologies. The needs of single photon detectors and other circuit components call up other materials such as phase change materials. Phase change materials has allowed emulating brain-like functions in a technologically affordable way, thus supporting developments in neuromorphic computation.[28] Alternative computing based on photonics offers a number of advantages. In particular, unlike most other qubits, photons do not suffer from decoherence and it is possible to use linear circuits to perform quantum computing. An 8-qubit quantum processor has been already reported in an integrated quantum photonic circuit.[29] The main material under investigation remains silicon for its versatility and scalability,[30] although integration based on III-V semiconductor is becoming very well established, especially for the generation of entangled photon pairs.[31]

One of the roadblocks in quantum photonics for computation has been the single photon detector. However, with a hybrid approach for near-IR single photon detector based on 100 nm wide superconducting nanowires[32] a dramatic advance is in sight. Nevertheless, there are several challenges remaining: quantum photonic circuits need to be architecture independent (quantum gate

26 Quantum Technologies Manifesto, May 2016 http://qurope.eu/system/files/u7/93056_Quantum%20Manifesto_WEB.pdf, accessed on 29thApril 2018.

27 https://ec.europa.eu/digital-single-market/en/news/intermediate-report-quantum-flagship-high-level-expert-group, February 2017, accessed on 29th April 2018.

28 Z. Cheng et al., On-chip photonic synapse, Sci. Adv. 3 (2017) e1700160.

29 J.W. Silverstone et al., On-chip quantum interference between silicon photon-pair sources, Nature Photonics 8 (2013) 104.

30 A. W. Elshaari et al, On-chip single photon filtering and multiplexing in hybrid quantum photonic circuits, Nature Comms. 8 (2017) 379.

31 J. Belhassen et al., On-chip III-V monolithic integration of heralded single photon sources and beam splitters, Appl. Phys. Lett. 112 (2018) 071105.

32 See, for example, W.H.P Pernice et al., High-speed and high-efficiency travelling wave single-photon detectors embedded in nanophotonic circuits, Nature Comms. 3 (2012) 1325.

Quantum Photonics

circuit diagrams), platform independent and foundry independent (silicon photonic circuits). See Fig. II.8.3.

Competitive situation of Quantum photonics

Europe has a leading position in Si-based quantum photonics and state of the art research in phase-change material nanophotonics. III-V semiconductor-based quantum photonics is also becoming rapidly established. China has a very strong position in quantum photonics and is making substantial investment to take the lead. The USA, Australia and Japan are focusing their efforts in alternative quantum platforms such as superconductors and solid-state systems.

In the EU, France, Germany, Sweden, Italy, Austria and the UK, amongst others, have all well-established quantum photonics research communities, often collaborating in international research projects.There has been a substantial amount of investment from industry in the last few years worldwide. Google, Microsoft, IBM, HP, Toshiba and Intel are all working in different implementations of quantum computing. Recent investment in Quantum Technologies has also driven a substantial increase in quantum start-ups. One of the latest developments is the 2.7 US$ billion investment announced by Canada on quantum radar technologies[33].

33 http://www.digitaljournal.com/tech-and-science/technology/canada-invests-2-7-billion-in-quantum-radar-technology/article/520808. Accessed on 29th April 2018.

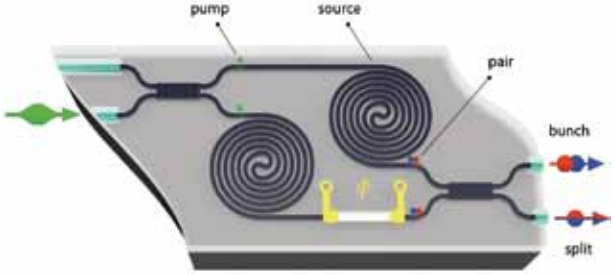

Fig. II.8.3: Schematics of a component in an integrated circuit: Identical spontaneous four-wave mixing (SFWM) photon sources for quantum photonics (Courtesy of Dr. Joshua W. Silverstone, University of Bristol).

Recommendations for Quantum photonics

Quantum photonics benefits from the development of quantum technologies in general, and integrated photonics in particular. Quantum photonics is one of the best-supported quantum technology platforms in Europe and the effort has to be maintained/increased to compete with non-EU effort. Quantum photonic computers can be realised using Si-based integrated photonics devices of sufficient quality, but not enough high-quality photonic fabrication facilities are available in the EU. Large companies are able to address the technological challenges in quantum photonics independently. Alternatively, start-ups can effectively contribute to the development of quantum software (and algorithms) and solutions tailored for specific quantum platforms. The adoption of quantum photonic devices by traditional (non-quantum) industries is still limited by the TRL of the approach. However, first trials to exploit industrial scale CMOS platform in realisation of spin-qubits has recently been initiated.[34]

It can be argued that quantum technologies in general will need to investigate to what degree hybrid systems are suitable for specific computational tasks. For example, photos as quantum information transmitters, weakly interacting spins as memories, and superconducting nanostructures as quantum information processors.

34 https://www.mos-quito.eu/ .

Medium Term [+5 years] ●●●●●●+

Long Term [+10 years] ●●●●●●+●●●●●●

Key research questions/issues

- Photons do not suffer from decoherence so they are highly suitable for computing.
- Si-based quantum photonics can use linear circuits, e.g., 8-qubit processor demonstrated.
- Single photon detectors for Si quantum photonics, currently relying on hybrid III-V/Si detectors or superconducting wire detectors.
- Some photonic schemes require low temperature operation (2 K).
- Phase change photonics allow brain function emulation.

Application needs & Impact for Europe

- Quantum Computation.
- Secure data transfer.
- Neuromorphic computing and their applications (see Concept on Neuromorphic Computing).

Technology and design challenges

- More theory is needed to develop alternative architectures.
- Full integration of all components on a chip for quantum computing and phase change materials for opto-neuromorphic computing.
- Long-term stability of photonic schemes must be improved, especially concerning the phase change materials, which require high peak temperatures.
- Two-photon absorption losses in detectors need a speed vs loss compromise in optical switching.
- Development needed on the cooling system technology.
- Footprint and scaling challenges for phase change photonic computation.

Definition of FoMs or planned evolution

	2023	2026	20329
Quantum key distribution (bit rate/ distance)	5 Mb/s/100 km (combined with 100 Gbit/s classical communication)	10 Mb/s/100 km (combined with Tbit/s classical communication)	QKD networks
Single photon detector SPD: compromise between efficiency and speed	Single synapses with weights and STDP		
Photonic synapses			Photonic neural networks

Other issues and challenges

- Novel architectures and more algorithms that harness the possibilities of quantum computing are needed.
- WP5 Equipment and Manufacturing science: Photonics-related manufacturing lags behind that of nanoelectronics.
- Dedicated research infrastructure is needed or access to modern nanofabrication facilities.

Phonon, Brownian and nano-opto-mechanical computing

Phonons, the quanta of lattice vibrations, and thermal fluctuations are among the lowest energy carriers to be considered in information processing down to fractions of a meV. With some imagination, fluctuations can be thought of as low-frequency phonons, basically a kind of acoustic phonons. Acoustic phonons are the carriers of thermal energy in non-metallic solids. Brownian motion and fluctuations are also closely intertwined sharing randomness as one of their main characteristics. As physical dimensions decrease, the mechanical modes of a structure can couple to electrons and photons in what is known as nanomechanics[35] and optomechanics,[36] respectively. In the latter case the phonons involved are optical ones, although at room temperature the contributions from acoustic phonons cannot be neglected. State variables based on thermal, Brownian and nano(opto) mechanical concepts have been proposed for computation with a single type or coupled (hybrids) variables. The common driving force behind these research areas is to lower the power consumption in potential alternative computing schemes. Furthermore, an important emerging aspect is the role of phononics in addressing the heat dissipation of the current CMOS circuitry.

Phonons as a way to address thermal management

The first associations of thermal phonons in information processing are related to dissipation in signal transmission and conversion, and heat removal from the hot spots in components and circuits. Although various strategies are and have been tested, one trend is to use fluidics to cool circuits and components. However, as the internet of things develops with an increasing pace, emphasis is being increasingly placed on autonomous systems, which renders the cooling-with-fluids approach rather impractical. Thermal management has become one of the main issues regarding development of nanoelectronics devices and circuits. It is the overriding reason of why the upper limit for clock frequencies of the integrated circuits is set in practice to 5 GHz. Consequently, understanding the behaviour of thermal phonons in nanostructures, heat transport across interfaces and the potential role of surface phonon polaritons[37] in heat removal is crucial for trials to circumvent the "heat death". Nanoscale thermal transport is addressed under the umbrella of nanophononics[38].

Thermal (phonon)-based computation

From another perspective, phonons or heat can potentially be used for information processing if suitable designs and materials to realise non-linear and switching devices can be realised. The requirement is that the density of states or the available phonon modes do not overlap, enabling the heat flow in one direction between the materials but not in the opposite direction, leading to rectification. Thermal conductivity and temperature measurement techniques in the nanoscale are required but these are by and large insufficiently accurate and calculations are very much under development or controversial.[39] Temperature as information token has been proposed considering phonons as particles.[40]

Another approach based on stochastic thermodynamics of an open system, in non-equilibrium and using the Landauer principle, has shown that a non-equilibrium state can be considered as a resource for information processing.[41] Crucial in the description are the concepts of energy and entropy treated dynamically, with and without a driving force leading to the first connection showing that energy and or heat is information. Information can be stored and erased in finite times, and trade-offs are possible between accuracy and dissipation.

A comparison of phonons (TRL 1) and electrons (TRL 9) for computation shows that while the electron-based computing needs voltages of at least 0.5 V, phonons would need lower energies, closer to the average acoustic energy of a fraction of meV. However, regarding speed the thermal processes are much slower than electronic ones, unless ballistic phonon propagation can be used, as well as phase changes and fast switches, which are still in the laboratory-stage.

Brownian computing

Furthermore, based on thermal and statistical physics, in a process resembling a random walk, Brownian motion-like computation has been proposed.[42] This method utilizes signal fluctuations to search in an energy landscape. To use Brownian motion to compute, energy is needed to bias the computation forward or an increase in entropy. In a circuit this is equivalent to exploring the configuration space. A possible application is the use of Brownian circuits in future computers and neural networks. For the design of future computers, signal fluctuations, rather than being an impediment to be avoided at any cost, may be an important ingredient to achieve efficient operation.

Competitive situation of Phonon, Brownian and nano-opto-mechanical computing

Europe has probably the strongest but dispersed community in nano-scale thermal transport, near-field radiation and Brownian motion, together with a very strong theoretical community on statistical physics. The NEMS and quantum NEMS communities are still small, in particular the latter. It also has a leading community in the experimental front, developing new methods of measurements and tools for fabrication. The consolidation of the community is poor and is an obvious weakness.

Recommendations for Phonon, Brownian and nano-opto-mechanical computing

In heat transport in the nano-scale, NEMS and Brownian computing, the role of entropy must be taken into account vis-à-vis a measurand (energy? temperature?). Likewise, the community needs to become one that can discuss and make progress and advocate its case. Industry needs to be convinced of the value that this community can bring, especially in heat management in the near future and in sub-k_BT information processes in the long term.

35 A.N. Cleland, Foundations of Nanomechanics (Springer-Verlag, Berlin, Heidelberg, New York, 2003).
36 M. Aspelmayer, T. Kippenberg and F. Marquardt, Cavity Optomechanics, Rev. Mod. Phys. 86 (2014) 1391.
37 See, e.g., B. Song et al., Near-field radiative thermal transport: From theory to experiment, AIP Advances 5 (2015) 053503.
38 S. Volz et al. Colloquium: Nanophononics – State of the Art and Perspectives, Eur. Phys. J. B 89 (2016) 15.
39 For a recent review see, G. Fugallo and L. Colombo, Calculating lattice thermal conductivity: a synopsis, Phys. Scr. 93 (2018) 043002; G. Fugallo and L. Colombo, Corrigendum: Calculating lattice thermal conductivity: a synopsis, (Phys. Scr. 93 043002), Phys. Scr. 93 (2018) 059501.
40 N. Li et al., Colloquium: Phononics: manipulating heat flow with electronic analogs and beyond, Rev. Mod. Phys. 84 (2012) 1045.
41 See, e.g., M. Esposito and C. Van der Broeck, Second law and Landauer principle far from equilibrium, Eur. Phys. Lett. 95 (2011) 40004 and J. M. R. Parrondo, J. M. Horowitz and T. Sagawa, Thermodynamics of information, Nature Physics 11 (2015) 131.
42 See, e.g., J. Lee et al., Brownian Circuits: Designs, Int. Journ. of Unconventional Computing 12 (2016) 341.

Phonon, Brownian and nano-opto-mechanical computing

Medium Term [+5 years]

Long Term [+10 years]

Key research questions/issues

- Potential for energy conversion in the nano-scale near-field radiative heat is not yet tested, except in realisations of surface-phonon polaritons but not in a sufficiently wide range of technological-relevant materials.
- Surface-phonon polaritons shown to transmit thermal energy over 100 µm's on the surface.
- To what type of interfaces does the concept of surface-phonon polaritons apply?
- What are the boundaries and implications of signals performing a random search, in Brownian computing, looking for a way out in a maze of a circuit determined by topology?
- What are the boundaries and implications of disorder-induced Anderson localization in the context of Brownian computing?
- Brownian computing has demonstrated the use of fluctuations in circuits based on SETs, through a random search mechanism, in addition to counting, testing of conditional statement, memory and arbitration of shared resources. Can an alternative to SETs be found?
- How large must the thermal driving field (driven fluctuations) be compared to the signal level?
- How to define an operational local temperature in the nano-scale under non-linear conditions?
- How does entropy change with varying distance between nanogaps and how important is it?
- Potential to reach THz in NEMs-based computing with low power operation.

Application needs & Impact for Europe

- Surface-phonon polaritons applied to enhance efficiency of thermal photovoltaics, magnetic switching and phase changes.
- Design of future computers and neural networks.
- Potential to lower power consumption by harvesting fluctuations.
- Brownian motion is used in less complicated device and to obtain universality.
- Harvest fluctuations instead of fighting them for computing (entropy-based computing?).
- NEMs-based concept could deliver cooling solutions by enhancing efficiency via driving the TE generator.
- Integration with spintronics.
- Potentially ultra-sensitive NEMs-based sensors.

Technology and design challenges

- Can we attempt evanescent wave engineering?
- What are the tolerances of thermal energy and fluctuation-based components and circuits?
- Other schemes to apply the concepts of NEMs-generated thermoelectricity?
- How to reach the ground state to move to quantum computation?
- Scalability?
- Need for ultra-clean devices.
- Control of nanoscale motion.
- Do we have a better chance with hybrid computation using one or more of these approaches?

Other issues and challenges

II.7 Manufacturing & Equipment and II.6 System Design and Heterogeneous Integration.

Definition of FoMs or planned evolution

	2023	2026	2029	2033
Thermal/phonon computing (low energy)	Define theoretically and experimentally energy cf. existing and new parameters. Relation between energy = $C_g(V_{dd})^2 = (k_B T \ln 2)/100$ for one bit of information demonstrated.			
Brownian/entropy computing, theory, algorithms, proof-of-concept	Simulation of simple information processes	First algorithms for programming	Circuit level proof-of-concept with specific functions.	Proof-of-concept realisation.

Synergies with other topics

The production processes and processing equipment of nanoelectronics circuits have been developed to the ultimate level at the sub-nm dimensions with hundreds of lithography steps on 300 mm wafers. The majority of the Beyond CMOS devices can benefit from the existing technology. The palette of materials will be broader but the compatibility of the new materials with the current processes is controllable. This aspect has to be discussed in collaboration with the II.7 Manufacturing & Equipment.

The majority of the new computing paradigms are based on non-von Neumann architectures. The design of the circuits, their architectures and connectivity to the CMOS platform, internet, telecom etc., have to be standardised and this has a close connection to II.6 System Design and Heterogeneous Integration.

Recommendations for Beyond CMOS

The Beyond CMOS chapter covers several rather different emerging technologies and alternative information processing paradigms, consequently it is challenging to compile comprehensive recommendations applicable to all the emerging technologies. Thus, below a succinct recommendation for each of them.

Tunnel FETs have the advantage to be compatible with the current von Neumann architecture. Moreover, TFETs have a high potential to low power operation. The main challenge is to improve the current carrying capacity to increase the operation speed. For this further development of material properties, their interfaces and, possibly, new device geometries are needed.

Neuromorphic computation holds a high promise in applications in applications for the IoT and in handling big data. It is making longer-term inroads in dedicated hardware and algorithms. There are several technology candidates and the planned FET CSA on neuromorphic computation may well accelerate the current progress

in the Brain flagship, in the ICT LEIT projects and future project constellations. Continued support is recommended.

Parts of spintronics are already commercialised in, e.g., memories. The longer-term target is to use pure spin waves or magnons in interconnects and signal processing to realise a very low power, compact and fast technology for ICT. Although increasing in maturity are topological insulators, these should be included due to their potential to enable robust signal routing. The challenge is to realise methods for spin wave generation, device structures to implement logical functions and algorithms development. Regarding topological insulators, a great deal of function-oriented material research is needed.

Si-based quantum photonics must be an integral part of the Quantum Technology flagship building on the European leadership in the field. Si quantum photonics is already pushing the frontiers of chip-level integration and competing globally in innovations, for example, with nanophotonics-based components such as single photon detectors-based on phase change materials.

The challenge due to heat dissipation is common to all information processing approaches. Silicon CMOS technology is currently dealing with it mainly by tolerating the wafer real state cost of "dark silicon" and limiting the frequency of operation to the low GHz range. A common thread running through most of the alternative computing approaches is the need to understand at conceptual, experimental and technological levels the thermal properties of materials and interfaces, and the energy flows in signal processing events. Consequently, understanding and controlling dissipation is crucial, not only for thermal and entropy computing, but also for all the emerging technologies, especially for the current CMOS technology and architectures.

The range of materials under investigation within alternative computing paradigms goes well beyond silicon, e.g., in quantum (nano)photonics, neuromorphic computing and spintronics. Steep slope devices are not an exception. Thus technological advances are urgently needed with figures of merit for several non-silicon based materials, ranging from scalable material production technologies, through wafer-scale nanofabrication with innovative tools and, last but not least, a combined effort from the start of the research with the design and architecture community.

A common factor affecting most of the alternative computing paradigms and Beyond CMOS technologies is the impact of nanofabrication in variability of critical dimensions and processing defects in the material. This requires novel approaches to dimensional, and possibly chemical, nanometrology. New nanometrology concepts, are needed accompanied by a traceable measurement protocol and appropriate and or novel instrumentation. A recommendation is to encourage the European Metrology Programme for Innovation and Research (EMPIR) program[43] to launch a call with the nanometer in mind specifically for ICT –Beyond CMOS applications. Alternatively, to ensure that traceable nanometrology becomes an integral part of all Beyond CMOS Nanoelectronics projects.

A critical issue for Europe with most of the Beyond CMOS and alternative computing concepts is the need for a dialogue between academia and industry to identify topics and concepts the exploration of which would be beneficial to European society and economy, despite the time scales governing their respective activities. In the US the Semiconductor Industry Association (SIA) lists Research under its priorities and policies[44] and the Semiconductor Research Corporation started a program on Nanoelectronics Computing Research (nCORE)[45] to "Explore fundamental materials, devices, and interconnect solutions to enable future computing and storage paradigms beyond conventional CMOS, beyond von Neumann architecture, or beyond classical information processing/storage", i.e., TRL 1 and 2 de facto included. Europe, which now has a research program in defence in addition to a focus on the Digital Economy[46], cannot afford to be dependent on foreign technology in which Beyond CMOS is likely to play a pivotal role in the medium and long terms. The investments in nanoelectronics and related R&D by the PPP ECSEL are in the few billion euros supporting mainly high TRL developments. It is recommended to set up efficient and dynamic instruments to enhance the dialogue between researchers in academia (specially researchers active in the Excellence Science pillar) and in visionary industries to explore the up-take of the emerging technologies. The leading Research Organisations ought to be part of the dialogue as their excellent infrastructure and extensive expertise will be pivotal for this endeavour. However, a spirit of cooperation in the low TRL research is needed, rather than competition within Europe. A second recommendation is that funding for TRL 1-2 level consortium-based research in, e.g, micro- and nanoelectronic technologies and (ICT-oriented) FET should be at least doubled in Horizon Europe. This would be an opportunity for the European nanoelectronics industry to secure a leading position in the ever-tightening global competition in the ICT markets of today, tomorrow and after tomorrow.

43 https://www.euramet.org/research-innovation/research-empir/.

44 https://www.semiconductors.org/issues/research/research/ accessed on 01 may 2018.

45 https://www.src.org/program/ncore/ accessed on 01 May 2018.

46 Research and Innovation: ICT projects in Horizon 2020, http://ec.europa.eu/information_society/newsroom/image/document/2018-20/7_desi_report_research_and_innovation_-_horizon_2020_E2357526-A51E-DCAD-71343D67E1A6B0A1_52242.pdf

III.1 General Recommendations

The aim of future research activities in the field of Nanoelectronics is to further develop Europe's S&T excellence to support technology development and innovation and strengthen its competitiveness and the market leadership of the related industries. Research and innovations in Nanoelectronics, covering the medium to long-term impacts, are crucial to the European technological leadership in ICT. They are complementary to ECSEL activities mainly devoted to short term applications.

The main recommendations for the nanoelectronic Technologies covered by NEREID are mentioned below:

For Advanced Logic and Memories

In the More Moore field, there are also strong interests in Europe for specific activities dealing with very low power systems, leading to possible disruptive applications for instance for future IoT systems, for embedded memories, for 3D sequential integration, or for application driven performance, e.g. high temperature operation for the automotive industry using for instance FD-SOI.

- For Nanowires, identify the best material and geometry options for logics (high-speed as well as low-power), develop millimeter wave front-ends with III-V MOSFETs (applications for communication, radar), and consider the 3D aspects of processing
- For FD SOI, develop differentiated options (RF, Embedded Memories, Imaging or molecules sensors) on FD-SOI (applications for automotive, IoT, smart sensors…), ULP design (V_d< 0,4 V) for IoT market (wearable, medical…), and 3D integration for future neuromorphic and quantum computing approaches
- For FinFET, develop co-integration of different channel materials, low contact resistivity and high strain solutions, improve finFET analog performance
- For NCFET, identify the maximum switching speed, the optimal dimensions, develop thin Hafnium based Ferroelectric layers, investigate the scaling potential of the device
- For CNTFET, develop solutions to lower the Schottky barriers at source/drain, to remove the metallic CNTs, faster growing process, design strategies to deal with variability induced by m-CNTs and doping fluctuation
- For Memories:
  - OxRAM, HRS broadening is the Challenge. New materials, new programming schemes need to be investigated
  - CBRAM, same as OxRAM plus a special focus on data retention, which is probably the most challenging topic for CBRAM
  - PCM, needs to progress on integration, necessary for GST patterning. In addition, material research needs to be continued to optimize data retention for scaled nodes
  - MRAM, etching, thus integration, problems can be much harder to solve than expected. The high current consumption can be a serious drawback for real applications, in particular for IoT
  - FeFET, widen the material screening in addition to the standard Si:HfO_2. A lot of work is necessary on the interface between channel and Fe layer.
- For 3D sequential integration, define which applications will benefit from very high density interconnections (IOT, neuromorphic…), and develop a 3D place and route tool
- For Modelling/Simulation, Characterization and Reliability, develop new tools taking into account all the new materials, technologies and device architectures in order to speed-up technology optimization and reduce the cost of technology development.

For Connectivity

Antennas & Passives

On demand Re-configurable and tunable Antennas and Passives, very compact and massive MIMO antennas, with beamforming systems and very high antennas' directivity for all the used band, 0-6 GHz and mmW. Work may address metamaterials, NEMs, MEMs and integrated passives technologies, packaging and modules, design, systems and microsystems.

Transceivers & Front End Radio

High Data Rate

Up to 100 GHz and up to THz Transceivers, stable and accurate local oscillators, and antennas' interfaces targeting high and agile spectrum usage, with wider communication bands, allowing Full-duplex communications and solving Interference management, with on-demand new PHY waveforms generation. Work may address New generation of nm CMOS, beyond CMOS, and mixed Silicon-III-V technologies, NEMs, MEMs, and new physics devices, combined with new design methodologies, modelisation and wireless long range, short range or wave guided systems.

Low Power Radio

Ultra-low power transceivers for WSN and IoT Networks, with µW consumed power objectives. Work may address Wake-Up Radio, ultra-stable ultra-low power time reference, charge transfer, or time-frequency modelisation and design methodologies, CMOS, Beyond CMOS, NEMs MEMs, and new physics devices, wireless, including ultrasonic, or silk guided systems.

Wireline

Low cost 1300 nm and 1500 nm laser sources, optic modulators, LEDs, and PIN diodes, with their electrical interfaces, drivers and Trans impedance receivers, for modulations giving 400 Gbs to Tbs. Work may address photonics integrated components, including laser and VCSELs, copper wireline interfaces, 3D packaging methodology, multiphysics modelisation and simulations, CMOS beyond CMOS, and low cost exotic More than Moore processes.

For Smart Sensors

General recommendations for the smart sensors in the automotive and in the medical/ healthcare segment described previously are the following one:

• Shared manufacturing infrastructure cost with other applications (e.g. between automotive and consumer), improved processes that further lower cost (like CMOS MEMS) or the creation of new devices with added value (e.g. software embedded within the sensor to deliver higher level functions) are some ways to improve margins as for example in MEMS market.

• CMOS integration, compatibility and readout circuitry. New enabling technologies keep coming. However, integration becomes more challenging and reliability gets less predictable. It is predicted that smart sensors will remain as close as possible to CMOS standards.

• Stability and reliability are the two most important features for the industrial take up of smart sensors. High reproducibility, ppb detection limits due to concentration, signature for functionalization, form factor and the power consumption of the platform are secondary characteristics that have to be taken into consideration for the

sensor development. As mentioned already, selectivity is not the most important feature for sensing.

• Regulations and guidelines are required to limit vehicle emissions and thus further reduce pollution and dependence on oil, to stablish emission standards that dictate the limits of pollutants (CO2, NOx, etc.) in indoor and outdoor air environments. Vehicle safety regulations are also a priority for Europe to reduce 50% of road accidents (cars, bicycles, pedestrian, etc.) by 2030. On the other hand, the different regulations and languages among national health organization are not helping to develop the medical market in Europe. Medical devices development including market introduction is very long (minimum 10 to 15 years), expensive and difficult nowadays, related to the long and tedious development stage, followed by the high cost of clinical validations, and the difficult process of CE labelling / FDA approval in case of novel device concepts (non-standard validation tests). The creation of a European excellence consulting and advising clinical validation centre would support the development of novel medical devices and reduce the time to market for them.

• Assembly testing, standards and metrology are crucial for the future success of smart sensors. There is a lack of metrology standards, commonly is difficult to interpret and it results in time consuming investigations.

• Auto-calibrated, self-calibrated or an easy way of sensor calibration is not a common feature for the sensors in the market yet. However, this is highly interesting and required for future industrialization and a long-term sensor stability. As an example, CMOS capacitive sensors have the advantage that they do not need to be calibrated but it might have a poor sensitivity.

• The maturity level of each sensor technology has to be assigned, estimating that a technology with a TRL higher than 6 would result in a product into market in less than 3 years approximately. The standards will be pushed very high in the different road-mapping but without excluding any technology for the next 10-year long term projection. The reason is that some application domains need mostly performance as in military while for others the cost is the most important factor or the repeatability, stability, reliability and yield for huge volume productions. A clear TRL correlation with technologies need to be established.

Thus, some of the smart sensor identified gaps by 2030 concern: manufacturability and cost (hybrid integration), low power consumption (energy efficiency), robustness of design and in production, and reliability.

For Smart Energy

Apart from WBG device development the WBG system integration is necessary to exploit the full potential.

- Packaging and system integration technologies enabling low parasitic inductances to master EMC issues
- Packaging and system integration technologies enabling reliability at higher temperatures
- Handling higher voltages on package/module level and system level: SiC in medium voltage (MV) applications e.g. in traction and industry
- Low inductance packaging and integration technologies: power PCB with chip embedding, system-in-package (SIP), switching cell in a package
- Passive components for fast switching: mainly inductors, reduce losses at high switching frequencies, thermal management of (integrated) passives
- Characterization, testing, modelling and reliability analysis of WBG packages, modules and converters

For Energy for autonomous systems

In general, the development of applications is the key to success for EH. IoT and energy harvesting are application-driven today, so projects should mainly focus on the development of a complete application (from harvesting to the use case). Concerning the concepts covered in this roadmap (vibrational, solar, thermal, RF EH and power management), the improvement of their performance and efficiency is as important as the development of “green” materials, replacing toxic/rare materials used nowadays (lead based piezoelectrics, Bi2Te3 for thermoelectrics, rare earth based magnetic material, e.g. NdFeB, for electromagnetic conversion). The use of nanotechnologies is foreseen to increase the performance of all the concepts in general. Flexible and low cost approaches for wearable applications should be developed as well. Increasing the bandwidth at a low frequency target (below 100 Hz) will help to fit applications for vibration-based mechanical energy harvesters. Concerning indoor photovoltaic applications, adapted structures and materials (light intensity and spectra…) should be developed. Small comment here about RF. Concerning power management circuits, it would be key to investigate size reduction of inductors, to enhance the efficiency of inductor-less power converter circuit topologies, to develop planar alternative to inductors and to tune microelectronic process parameters and technologies to reduce leakage for reduced power consumption, allowing low input voltages.

For System Design and Heterogeneous Integration

In the following, the most important recommendations related to System Design and Heterogeneous Integration, emerged during the discussion in the working group, are summarised:

- Validation: which is the level of robustness that is acceptable, confidence => When is it done?
- Add Software in the middle, starting from the application;
- The value is not in the device itself, but in system integration and in the related data, the Information is at systemic level;
- Balance of how much happens at each node and the energy for transmission (for reliability/security reasons too);
- Where to position the intelligence;
- The future is to move from Embedded Computing to Embedded Intelligence;
- Definition of standards for interoperabilty. Openness of standard cannot prevent monetisation.
- Re-Usability / Reconfigurability
- Software-like re-programmability with (almost) hardware like efficiency
- Energy
  - Management
  - Consumption when is necessary only
  - Importance of categorizing the application in terms of Energy Boundaries
- Automated Design Space Exploration and Automated Design Decisions
- From Connected Devices to Distributed Embedded Systems (System of Systems) => Network Synthesis, Network is a Design Dimension
- Environment is Part of the System
- The aggregated results highlight the importance of the Sensor Fusion and Validation at system level, taking in consideration the environment where the system will operate (Environment-aware Design).
- The strategic conclusion is that it is for Europe a very good opportunity to drive an increase in System Knowledge. In Europe many important stakeholders are present, with original knowledge, bringing Europe to a leading position for System Level Applications.

For Equipment and Manufacturing Science

- Concurrent areas' (II.1 – II.6, II.8) were analyzing their domains in view of the presented applications and derive immediate and long-term requirements in terms of materials, processes and manufacturing needs.
- The feeling exists, that with the worldwide effort on materials, processes and manufacturing in the domain of More Moore, the imminent needs of European application domains is covered. However, more specific needs in the other NEREID domains were identified.
- In the II.7 roadmap activities were covered, where Europe is leading in terms of materials, processes and manufacturing, but where the demand from application side is stronger outside of Europe (e.g. EUV lithography equipment).
- Cover activities in II.7 where application wise Europe is leading, but where specific needs for materials, process and manufacturing require continued attention (e.g. OLED).
- Synergies with IRDS activities whenever possible, in particular for the section manufacturing science.

For Beyond CMOS

The Beyond CMOS chapter covers several rather different emerging technologies and alternative information processing paradigms, consequently it is challenging to compile comprehensive recommendations applicable to all these emerging technologies. Thus, below a succinct recommendation for each of them is given.

Tunnel FETs have the advantage to be compatible with the current von Neumann architecture. Moreover, TFETs have a high potential for low power operation. The main challenge is to improve the current carrying capacity to increase the operation speed. For this, further development of material properties, their interfaces and, possibly, new device geometries are needed.

In the near term, neuromorphic computation holds a high promise in applications in the IoT and big data applications. It is making longer-term inroads in dedicated hardware and algorithms. There are several technology candidates and the planned FET CSA on neuromorphic computation may well accelerate the current progress in the Human Brain flagship, in the ICT LEIT projects and future project constellations.

Parts of spintronics are already commercialised in, e.g., memories. The longer-term target is to use pure spin waves or magnons in interconnects and signal processing to realise a very low power, compact and fast technology for ICT. Although further ahead in maturity are topological insulators. They should be supported due to the potential to enable robust signal routing. The challenge is to realise methods for spin wave generation, device structures to implement logical functions and algorithms development. Regarding topological insulators, plenty of function-focused material research is needed. This is an excellent opportunity for Europe to take the lead in topological matter applications.

Si-based quantum photonics must be a strong integral part of the Quantum Technology flagship building on the European leadership in the field. Si quantum photonics is already pushing the frontiers of chip-level integration and competing globally in innovations, for example, with nanophotonics-based components such as single photon detectors-based on phase change materials.

The challenge due to heat dissipation is common to all information processing approaches. Silicon CMOS technology is currently dealing with it mainly by tolerating the wafer real state cost of "dark silicon" and limiting the frequency of operation to the low GHz range. A common thread running through most of the alternative computing approaches is the need to understand at conceptual, experimental and technological levels the thermal properties of materials and interfaces, and the energy flows in signal processing events. Consequently, understanding and controlling dissipation is crucial, not only for thermal and entropy computing, but also for all the emerging technologies, and, especially for the current CMOS technology and architectures. This requires a resolute effort at European level to first build and consolidate the understanding and, in parallel, focus on facing the engineering challenges of ICT. For example, an immediate large action is needed in low power technology integratable with existing CMOS for IoT (e.g., microcontrollers) or specific applications and neuromorphic computing, from TRL1 to TRL5.

The range of materials under investigation within alternative computing paradigms goes well beyond silicon, e.g., in quantum (nano)photonics, neuromorphic computing and spintronics. Steep slope devices are not an exception. Thus technological advances are urgently needed with figures for merit of several non-silicon based materials, ranging from scalable material production technologies, through wafer-scale nanofabrication with innovative tools and, last but not least, a combined effort from the start with the design and architecture community.

A common factor affecting most of the alternative computing paradigms and Beyond CMOS tchnology is the impact of nanofabrication in variability of critical dimensions and processing defects in the material. This requires novel approaches to dimensional, and possibly chemical, nanometrology. Not only new concepts, since these need to be accompanied by a traceable measurement protocol and instrumentation, the latter being hardly existent. A possible recommendation is to encourage the European Metrology Programme for Innovation and Research (EMPIR) program to launch a call with the nanometer in mind specifically for ICT –Beyond CMOS applications.

Beyond CMOS and alternative computing concepts needs an increased involvement of the European industry in future European projects in this field in order to strengthen the ecosystem and technology transfer for speeding up technological innovation in Nanoelectronics. In the US the Semiconductor Industry Association (SIA) lists Research under its priorities and policies and the Semiconductor Research Corporation started a program on Nanoelectronics Computing Research (nCORE) to "Explore fundamental materials, devices, and interconnect solutions to enable future computing and storage paradigms beyond conventional CMOS, beyond von Neumann architecture, or beyond classical information processing/storage". In Europe the investments in Nanoelectronics and related R&D by the JU ECSEL is a few billion Euros but it supports mainly higher TRL developments. To develop the link between disruptive technology and applications, the funding of TRL 2-3 level research needs to be substantially increased. Being the first to develop and test novel concepts and secure the intellectual property on the next generation of technologies for e.g. the IoT, 5+G, artificial intelligence and environmentally sound ICT, would be an opportunity for the European nanoelectronic industry to secure a leading position in the ever-tightening global competition in the ICT market today and tomorrow.

Finally, the Beyond CMOS researchers in Europe need encouragement to explore application-driven routes, in parallel to carrying out excellence science. In that way Europe could capitalise the potential of Beyond CMOS ideas, structures and devices.

III.2 General Conclusion

The NEREID Project was very successful and led to an ambitious Nanoelectronic Roadmap including all the important technologies for many applications representing large future markets. The Nereid Roadmap took into account the specificity of the European industrial and academic landscape and will be very useful for equipment, semiconductors and application developments.

The project supported the participation of more than 100 application and technology experts, coming from leading research actors in industry and academia, to General and Domain Workshops. These Workshops allowed the consortium to better define the technology roadmap in terms of applications requirements (in the fields of Energy, Automotive, Medical/Life science, Security, IoT/Smart connected objects, Mobile convergence, Digital Manufacturing) and technology evolution (Advanced Logic and Connectivity, Functional diversification, Beyond CMOS, Heterogeneous Integration and System design, Equipment, Materials and Manufacturing Science), and to discuss the convergence between applications and technologies.

This common work between technology and application led to the early identification of the main challenges and the most promising technologies needing additional R&D activities, which will be very useful for the future electronic components systems of European companies leading to a strong impact on the European economy and society.

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